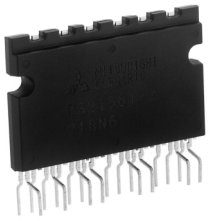
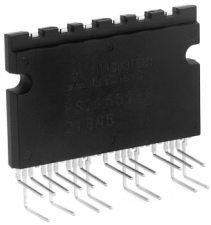
PS21661-RZ/FR

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21661-RZ **PS21661-FR**





INTEGRATED POWER FUNCTIONS

- 600V/3A low-loss 5th generation IGBT inverter bridge for 3 phase DC-to-AC power conversion.

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

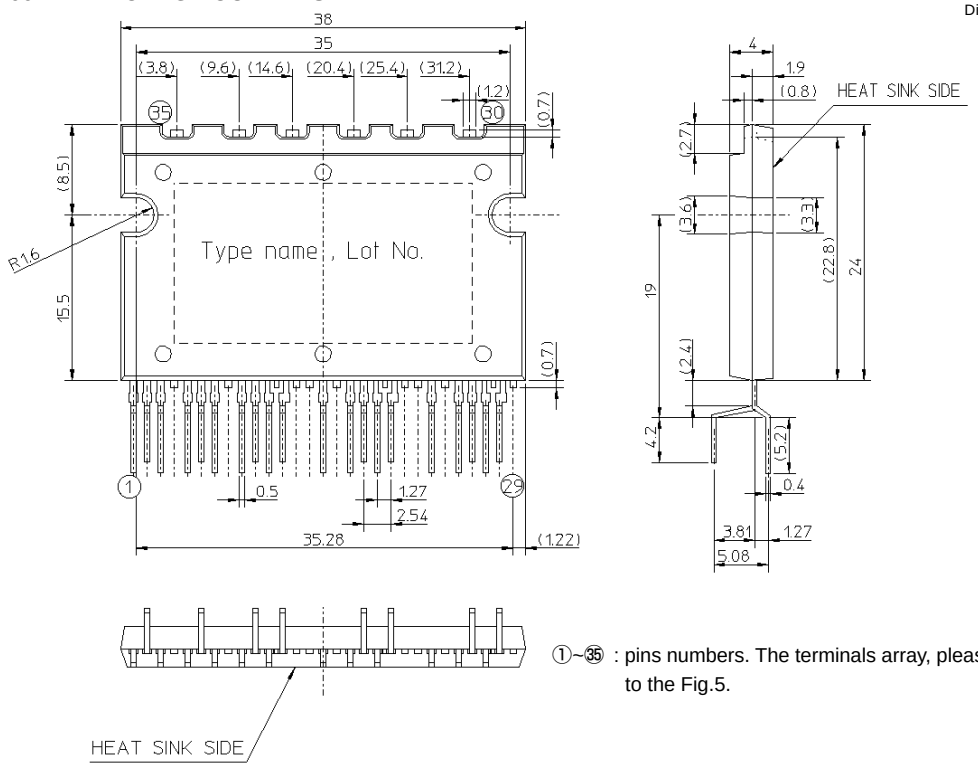
- For upper-leg IGBTs :Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage protection (UV).
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible Schmitt Trigger receiver circuit (Active high), Arm-short-through interlock protection.

APPLICATION

AC100V~200V, three-phase inverter drive for small power motor control.

Fig. 1 PS21661-RZ PACKAGE OUTLINES

Dimensions in mm

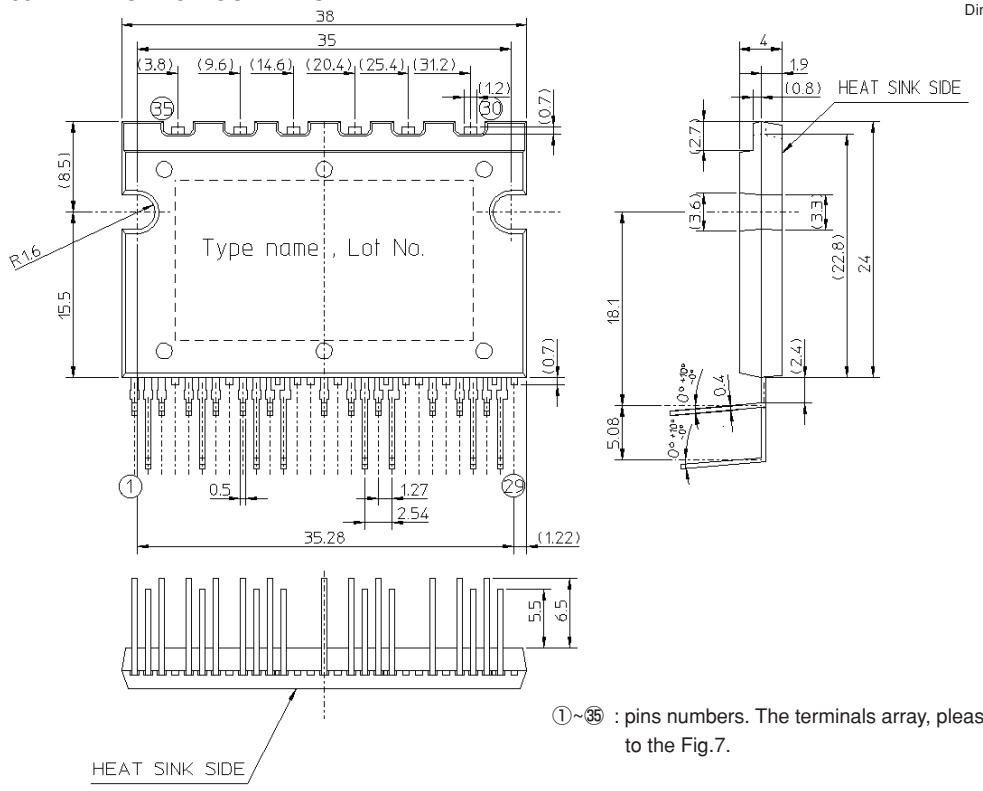


①~㉟ : pins numbers. The terminals array, please reference to the Fig.5.

MITSUBISHI ELECTRIC

Fig. 2 PS21661-FR PACKAGE OUTLINES

Dimensions in mm



①~㉟ : pins numbers. The terminals array, please reference to the Fig.7.

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-N	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-N	500	V
V_{CES}	Collector-emitter voltage		600	V
±I_C	Collector current	T_f = 25°C	3	A
±I_{CP}	Collector current (peak)	T_f = 25°C, tw ≤ 1msec	6	A
P_C	Collector dissipation	T_f = 25°C, per 1 chip	13.8	W
T_j	Junction temperature	(Note 1)	–20~+150	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the SIP-IPM is 150°C (@ T_f ≤ 100°C) however, to insure safe operation of the SIP-IPM, the average junction temperature should be limited to $T_{j(ave)}$ ≤ 125°C (@ T_f ≤ 100°C).

CONTROL (PROTECTION) PART

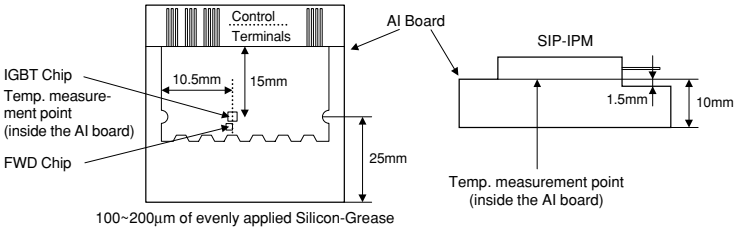
Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U (V_{UFS}), V_{VFB}-V (V_{VFS}), V_{WFB}-W (V_{WFS})	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}	–0.5~V_D	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	–0.5~V_D	V
I_{FO}	Fault output current	Sink current at F_O terminal	10	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	–0.5~V_D	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (short circuit protection capability)	V_D = 13.5~16.5V, Inverter part T_j = 125°C start, non-repetitive, less than 2 µs	400	V
T_f	Heatsink operation temperature	(Note 2)	–20~+100	°C
T_{stg}	Storage temperature		–40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	V_{rms}

Note 2 : T_f MEASUREMENT POINT

Al Board Specification : Dimensions 50 × 50 × 10mm, finishing 12s, warp –50~+100µm



100~200µm of evenly applied Silicon-Grease

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-f)Q}$	Junction to fin thermal resistance	Inverter IGBT part (per 1/6 module) (Note 3)	—	—	9.0	°C/W
$R_{th(j-f)F}$		Inverter FWD part (per 1/6 module) (Note 3)	—	—	9.0	

Note 3 : Grease with good thermal conductivity should be applied evenly about +100µm ~ +200µm on the contact surface of SIP-IPM and a heat-sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = V_{DB} = 15V, V_{IN} = 5V	I_C = 3A, T_j = 25°C	—	1.60	2.15	V
			I_C = 3A, T_j = 125°C	—	1.70	2.30	
V_{EC}	FWD forward voltage	T_j = 25°C, –I_C = 3A, V_{IN} = 0V		—	1.55	2.00	V
t_{on}	Switching times	V_{CC} = 300V, V_D = 15V, I_C = 3A, T_j = 125°C, Inductive load (upper-lower arm), V_{IN} = 0 ↔ 5V		0.35	0.70	1.10	µs
t_{rr}				—	0.20	—	µs
$t_{c(on)}$				—	0.35	0.55	µs
t_{off}				—	1.00	1.50	µs
$t_{c(off)}$				—	0.55	1.10	µs
I_{CES}	Collector-emitter cut-off current	V_{CE} = V_{CES}	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL (PROTECTION) PART

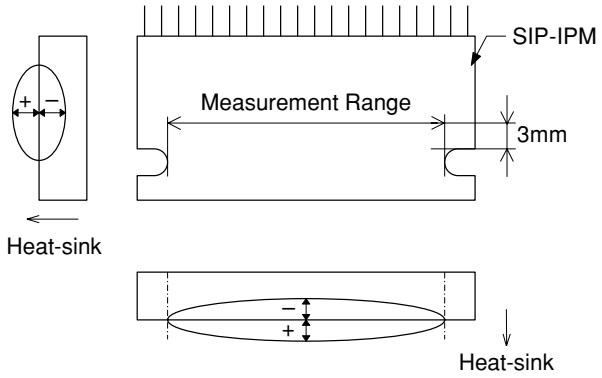
Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	V_D = 15V, V_{IN} = 0V	Total of V_{N1}-V_{NC} (U, V, W)	—	—	3.60	mA
		V_D = 15V, V_{IN} = 5V		—	—	3.90	mA
I_{DB}		V_{DB} = 15V, V_{IN} = 0V	V_{UFB}-U (V_{UFS}), V_{VFB}-V (V_{VFS}), V_{WFB}-W (V_{WFS})	—	—	0.50	mA
		V_{DB} = 15V, V_{IN} = 5V		—	—	0.50	mA
V_{FOH}	Fault output voltage	V_{SC} = 0V, FO circuit : 1kΩ to 5V pull-up		4.9	—	—	V
V_{FOL}		V_{SC} = 1V, I_{FO} = –10mA		—	—	0.95	V
I_{IN}	Input current	V_{IN} = 5V		0.70	1.06	1.50	mA
$V_{SC(ref)}$	Short circuit trip level	T_j = 25°C, V_D = 15V (Note 4)		0.43	0.48	0.53	V
UV_{DBt}	Supply circuit under-voltage protection	T_j ≤ 125°C	Trip level	10.0	—	12.0	V
UV_{DBr}			Reset level	10.5	—	12.5	V
UV_{Dt}			Trip level	10.3	—	12.5	V
UV_{Dr}			Reset level	10.8	—	13.0	V
t_{FO}	Fault output pulse width	(Note 4)		20	40	—	µs
$V_{th(on)}$	ON threshold voltage	Applied between: UP, VP, WP-V_{NC}, UN, VN, WN-V_{NC}		2.10	2.35	2.60	V
$V_{th(off)}$	OFF threshold voltage			1.10	1.40	1.80	V

Note 4 : Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 5.1A

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : (M3)	0.59	0.69	0.78	N·m
Weight		—	10	—	g
Heat-sink flatness	(Note 5)	–50	—	+100	μm

Note 5: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-N	0	300	400	V
V_D	Control supply voltage	Applied between V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U (V_{UFS}), V_{VFB}-V (V_{VFS}), V_{WFB}-W (V_{WFS})	13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation		–1	—	1	V/μs
t_{dead}	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through	1.5	—	—	μs
f_{PWM}	PWM input frequency	$T_j \leq 125°C$, $T_f \leq 100°C$	—	15	—	kHz
I_O	Allowable r.m.s current	V_{CC} = 300V, V_D = 15V, f_C = 15kHz, P.F = 0.8, sinusoidal $T_j \leq 125°C$, $T_f \leq 100°C$	—	—	1.5	Arms
V_{NC}	V_{NC} terminal voltage	Applied between V_{NC}-N (include surge voltage)	–5	—	5	V
t_{XX}	minimum on pulse width	U_P, V_P, W_P, U_N, V_N, W_N terminal	0.7	—	—	μs

Fig. 3 THE SIP-IPM INTERNAL CIRCUIT

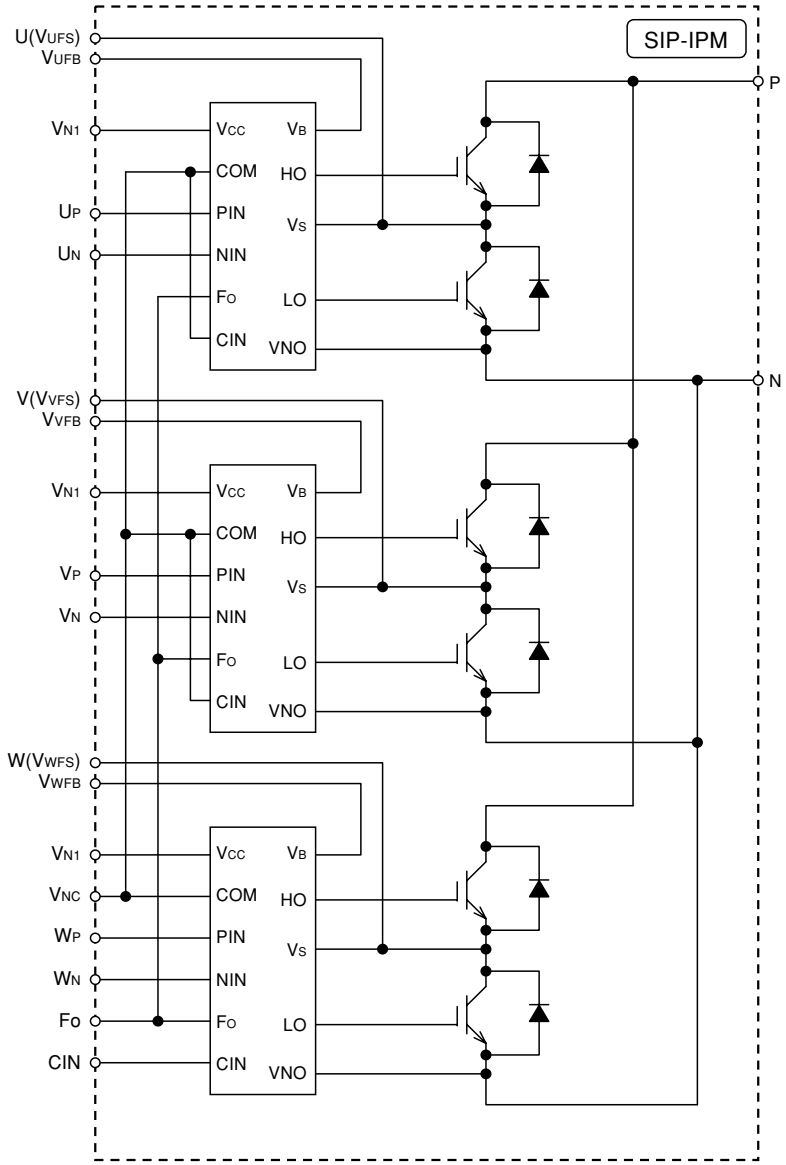
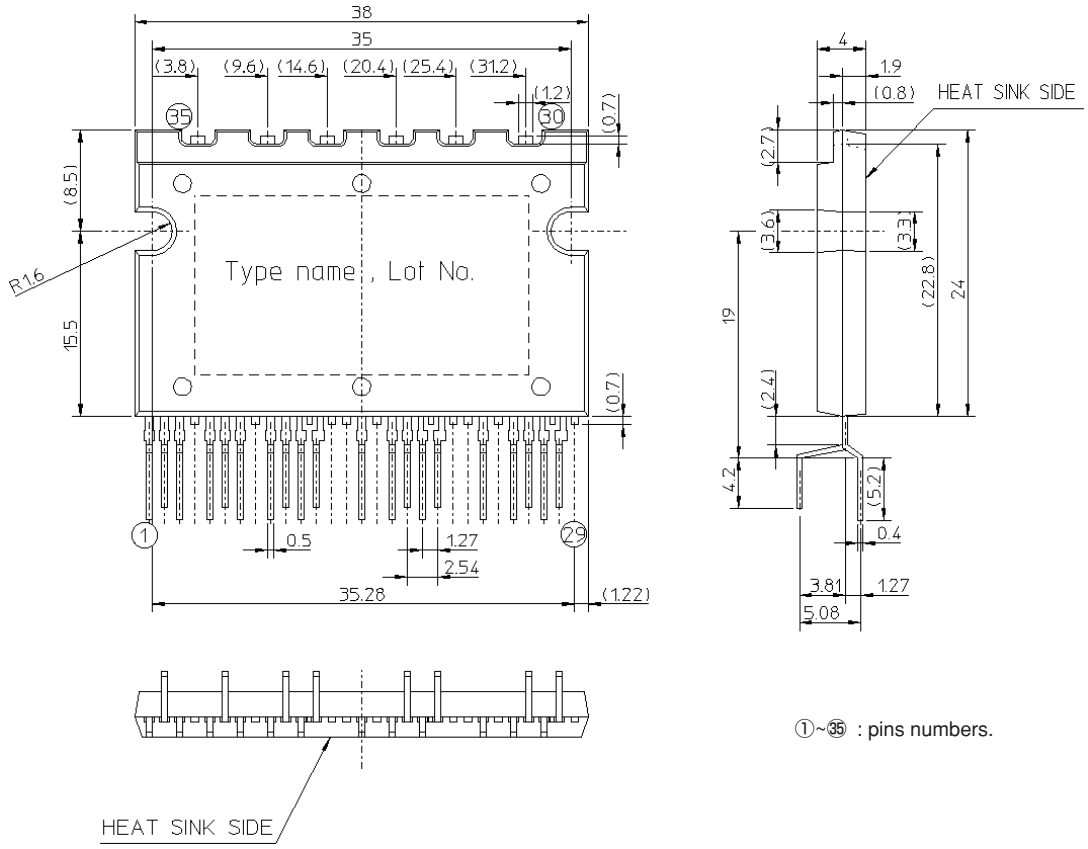


Fig. 4 PS21661-RZ PACKAGE OUTLINES



①~㉟ : pins numbers.

Terminal No	Symbol	Description
1	N	Inverter DC-link negative (GND) terminal
2	P	Inverter DC-link positive terminal
3	F_O	Fault output terminal
5	V_{NC}	Control GND terminal
6	CIN	Short-circuit trip voltage sensing terminal
7	V_{N1}	Control supply terminal
9	W_N	W-phase N-side control input terminal
10	V_{WFB}	W-phase P-side drive supply terminal
11	W_P	W-phase P-side control input terminal
12	W(V_{WFS})	W-phase inverter output terminal (W-phase P-side drive supply GND terminal)
15	V_{N1}	Control supply terminal
17	V_N	V-phase N-side control input terminal
18	V_{VFB}	V-phase P-side drive supply terminal
19	V_P	V-phase P-side control input terminal
20	V(V_{VFS})	V-phase inverter output terminal (V-phase P-side drive supply GND terminal)
23	V_{N1}	Control supply terminal
25	U_N	U-phase N-side control input terminal
26	V_{UFB}	U-phase P-side drive supply terminal
27	U_P	U-phase P-side control input terminal
28	U(V_{UFS})	U-phase inverter output terminal (U-phase P-side drive supply GND terminal)

The following pins are dummy pins are therefore should not be connected.
4,8,13,14,16,21,22,24,29,30~35 (30~35 are the high voltage side pins.)

Terminals array

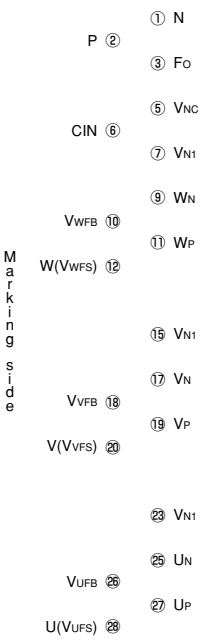
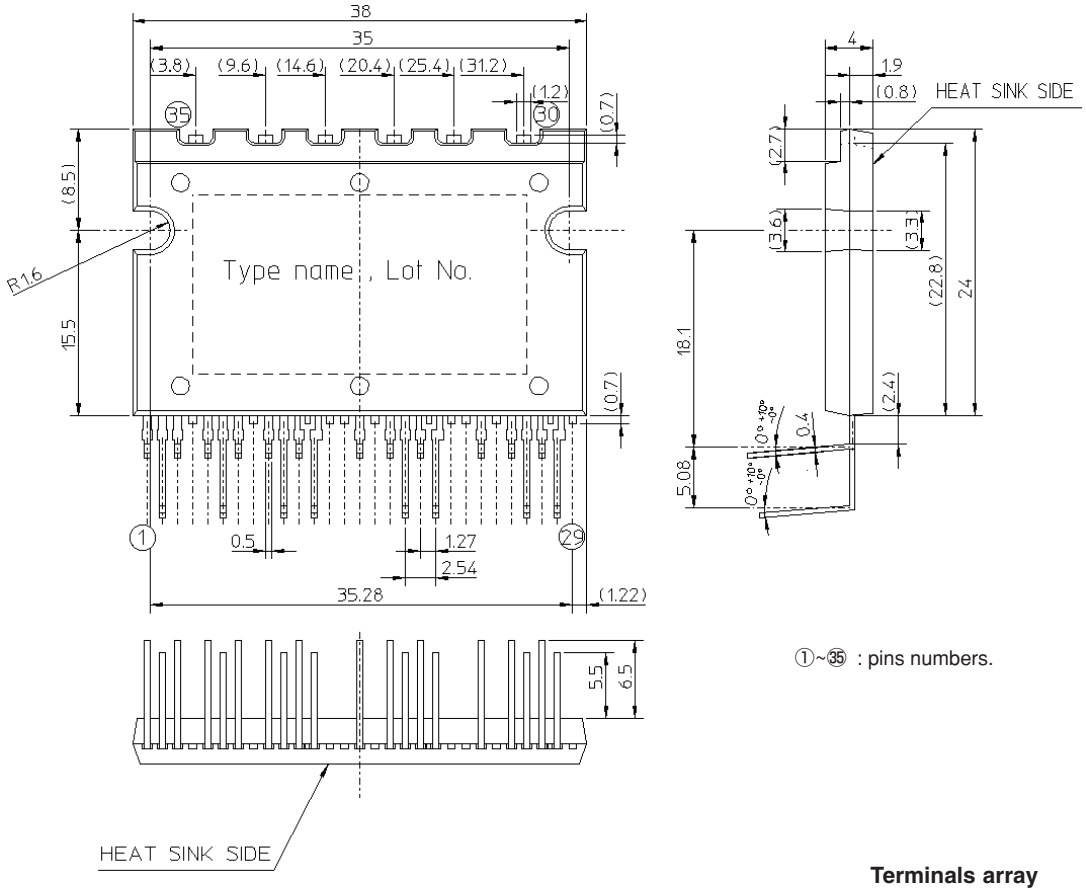


Fig. 5

Fig. 6 PS21661-FR PACKAGE OUTLINES



①~㉟ : pins numbers.

Terminal No	Symbol	Description
1	N	Inverter DC-link negative (GND) terminal
2	P	Inverter DC-link positive terminal
3	F_O	Fault output terminal
5	V_{NC}	Control GND terminal
6	CIN	Short-circuit trip voltage sensing terminal
7	V_{N1}	Control supply terminal
9	W_N	W-phase N-side control input terminal
10	V_{WFB}	W-phase P-side drive supply terminal
11	W_P	W-phase P-side control input terminal
12	W(V_{WFS})	W-phase inverter output terminal (W-phase P-side drive supply GND terminal)
15	V_{N1}	Control supply terminal
17	V_N	V-phase N-side control input terminal
18	V_{VFB}	V-phase P-side drive supply terminal
19	V_P	V-phase P-side control input terminal
20	V(V_{VFS})	V-phase inverter output terminal (V-phase P-side drive supply GND terminal)
23	V_{N1}	Control supply terminal
25	U_N	U-phase N-side control input terminal
26	V_{UFB}	U-phase P-side drive supply terminal
27	U_P	U-phase P-side control input terminal
28	U(V_{UFS})	U-phase inverter output terminal (U-phase P-side drive supply GND terminal)

The following pins are dummy pins are therefore should not be connected.
4,8,13,14,16,21,22,24,29,30~35 (30~35 are the high voltage side pins.)

Terminals array

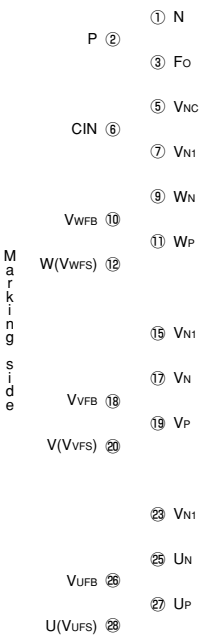
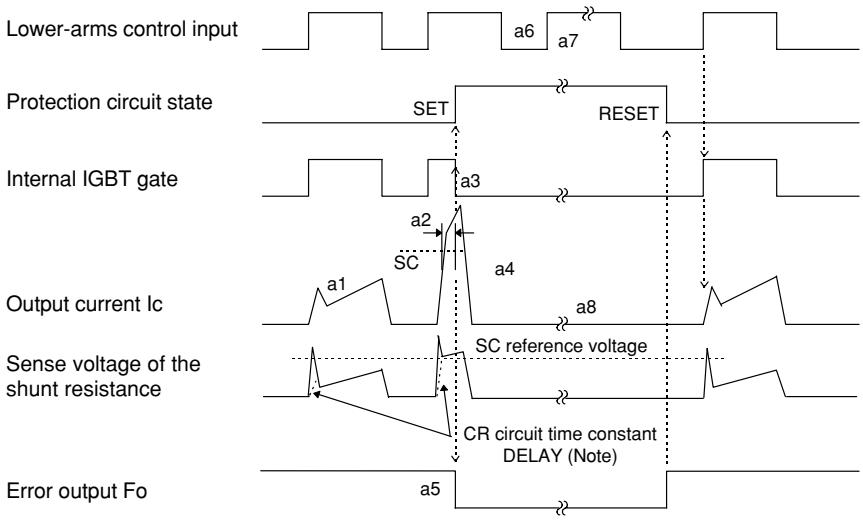


Fig. 7

Fig. 8 TIMING CHARTS OF THE SIP-IPM PROTECTIVE FUNCTIONS

[A] Short-Circuit Protection (Lower-arms only)

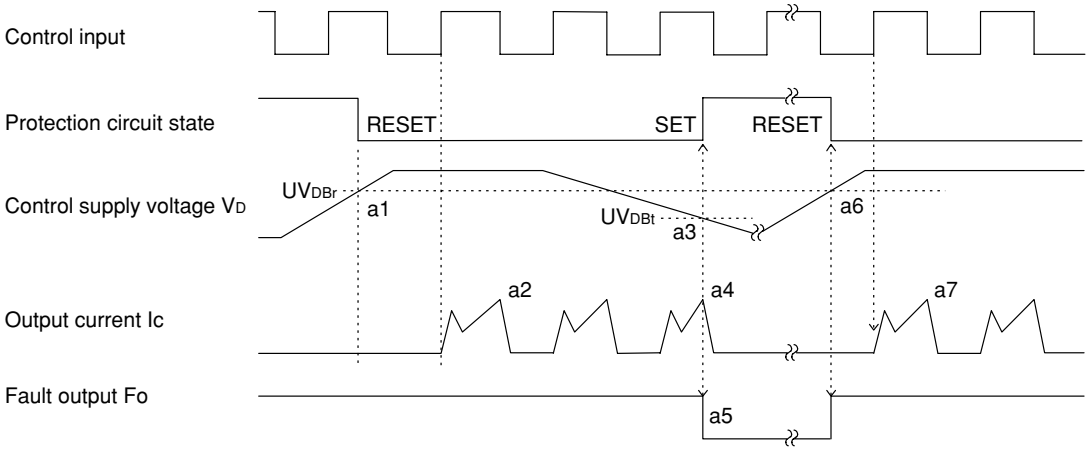
a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit current detection (SC trigger).
a3. Hard IGBT gate interrupt.
a4. IGBT turns OFF.
a5. FO output (20~80μs).
a6. Input "L" : IGBT OFF state.
a7. Input "H" : IGBT ON state, but during the FO active signal the IGBT doesn't turn ON.
a8. IGBT OFF state.



Note : The CR time constant safe guards against erroneous SC signal resulting from di/dt generated voltages when IGBT turns ON. The optimum setting for the CR circuit time constant is 1.5~2.0μs.

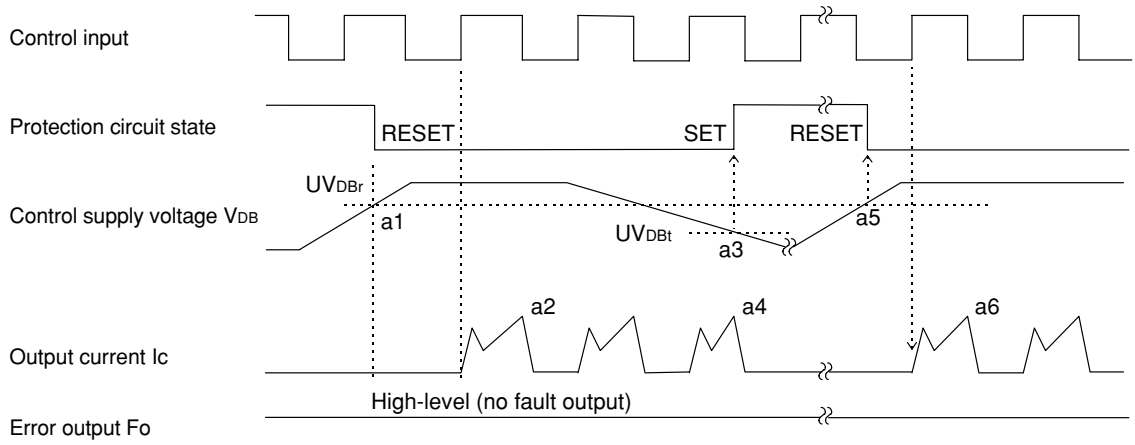
[B] Under-Voltage Protection (Lower-arms, UVD)

a1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when the next input is applied.
a2. Normal operation : IGBT ON and carrying current.
a3. Under voltage trip (UV_{Dt}).
a4. IGBT OFF in spite of control input condition.
a5. FO output (20~80μs).
a6. Under voltage reset (UV_{Dr}).
a7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-arms, UV_{DB})

a1. Control supply voltage rises : After the voltage level reaches UV_{DBr}, the circuits start to operate when the next input is applied.
a2. Normal operation : IGBT ON and carrying current.
a3. Under voltage trip (UV_{DBt}).
a4. IGBT OFF in spite of control input condition, but there is no F_O signal output.
a5. Under voltage reset (UV_{DBr}).
a6. Normal operation : IGBT ON and carrying current.



[D] Simultaneous input signal prevention function

a1 a3. Normal operation : IGBT ON and outputing IGBT gate voltage.
a2 a4. Normal operation : IGBT ON and outputing IGBT gate voltage.
a5. Abnormal pulse input.
a6. IGBT OFF state.
a7. No fault output.

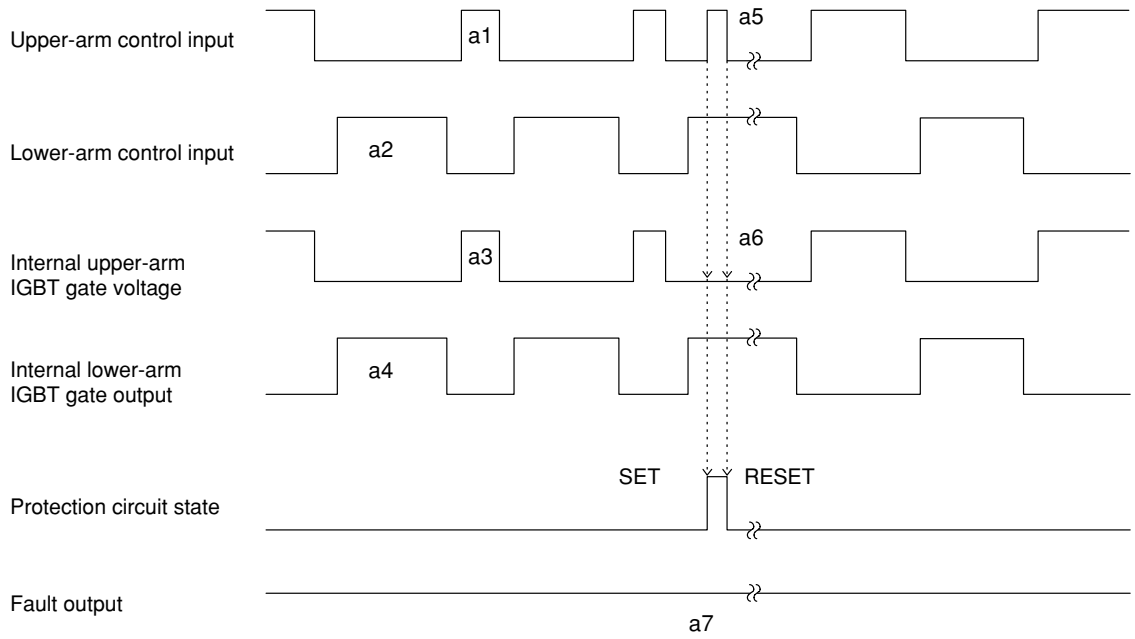
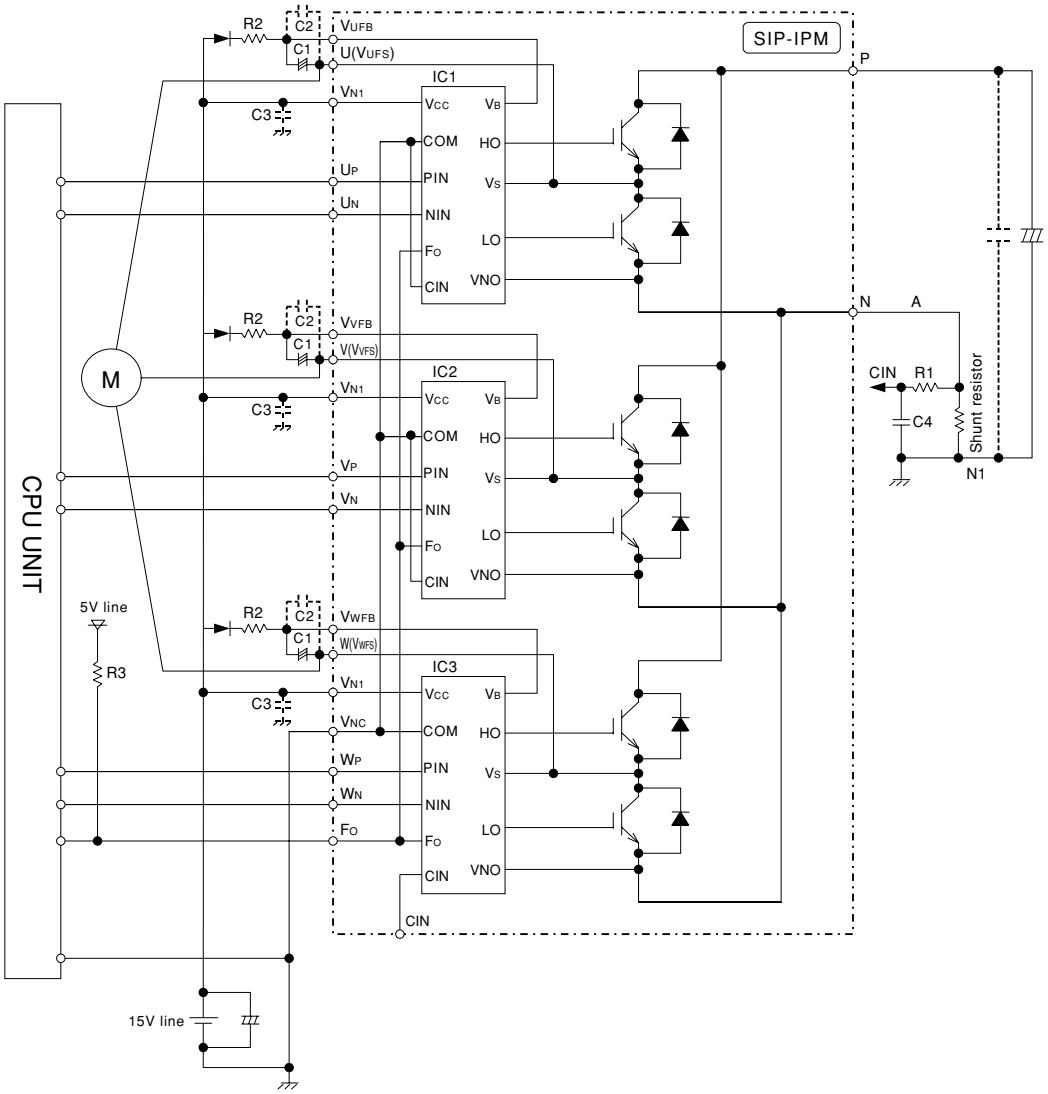


Fig. 9 TYPICAL SIP-IPM APPLICATION CIRCUIT EXAMPLE



Note 1 : Input signal lines are pulled-down with 4.7kΩ (min.) internal resistor. If these input lines are susceptible to noise, an RC coupling at each input is recommended. Input signal voltage is determined by the values of internal pull-down resistor and the external connected resistor. Set the external resistance value so that input signal voltage exceeds the on-threshold voltage. To prevent the input signals oscillation, the wiring of each input should be as short as possible.

2 : By virtue of integrating the specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3 : F_O output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 1kΩ resistance.

4 : Approximately a 0.1~2μF by-pass capacitor should be used across each power supply connection terminals.

5 : To prevent errors of the protection function, the wiring of A should be as short as possible.

6 : Each capacitor should be located as close to the pins of the SIP-IPM as possible.

7 : In the recommended protection circuit, please select the R_1C_4 time constant in the range of 1.5~2μs.

8 : To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P&N1 pins is recommended.