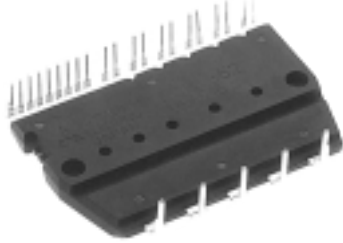


# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

## PS20341-N



### INTEGRATED POWER FUNCTIONS

500V/3A low-loss 4th generation (planar) IGBT inverter bridge for 3 phase DC-to-AC power conversion.

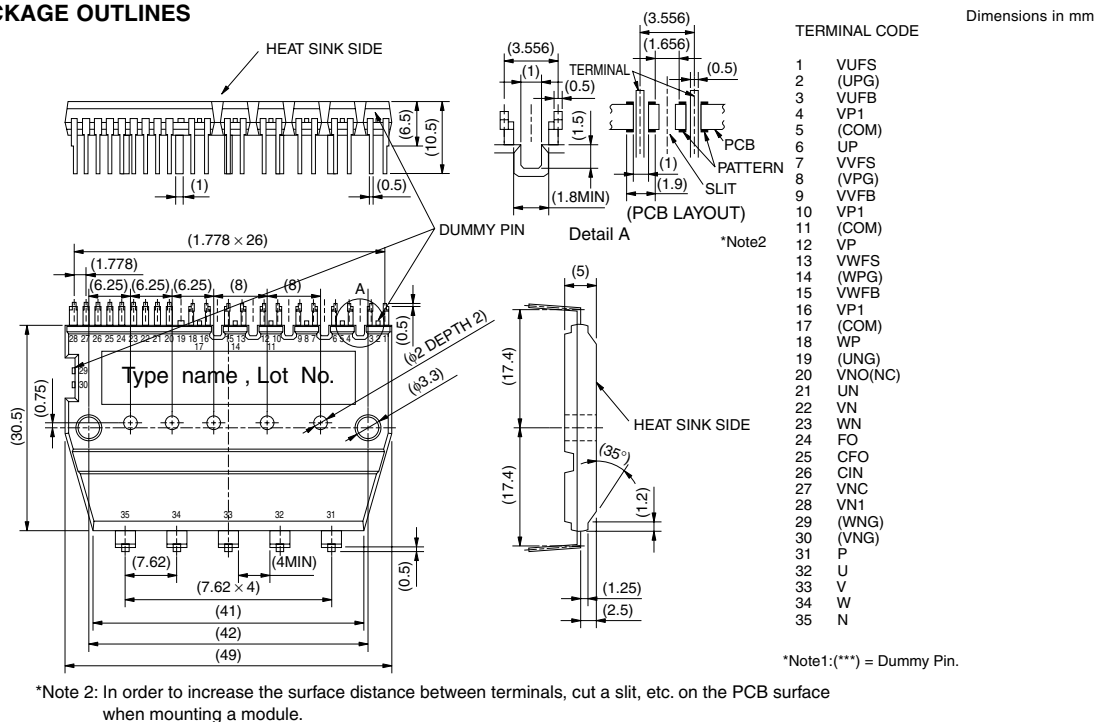
### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.  
Note : Bootstrap supply scheme can be applied.
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short-circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side IGBT).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

## APPLICATION

AC100V~200V inverter drive for motor control.

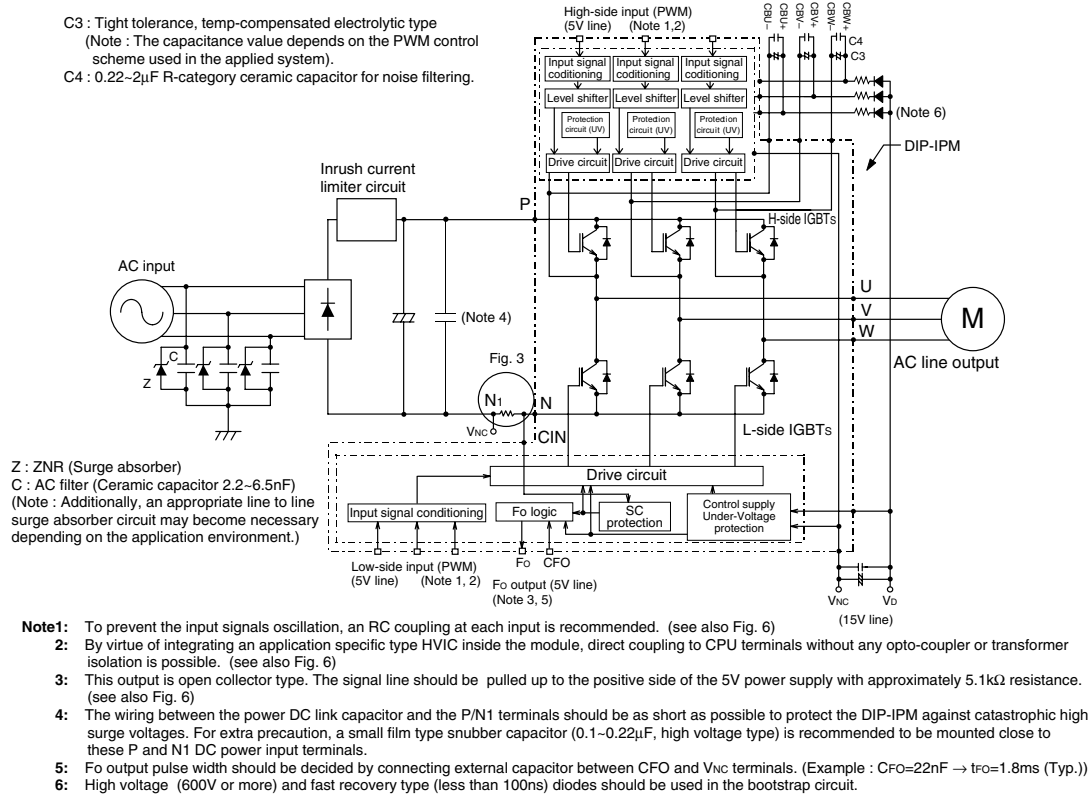
Fig. 1 PACKAGE OUTLINES



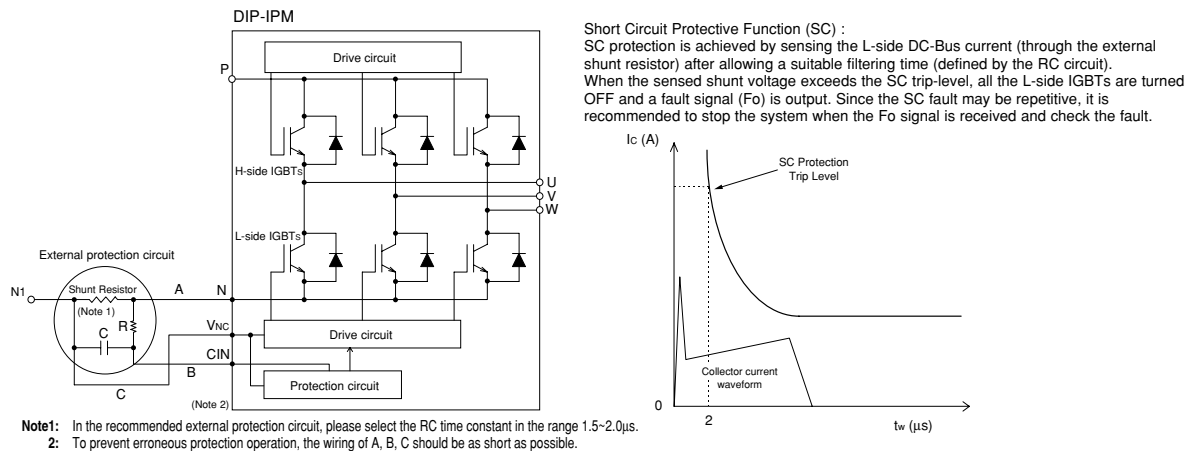
# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

**Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)**



**Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT**



# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

## INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	350	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	400	V
VCEs	Collector-emitter voltage		500	V
$\pm I_C$	Each IGBT collector current	$T_f = 25^\circ\text{C}$	3	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_f = 25^\circ\text{C}$ , instantaneous value (pulse)	6	A
Pc	Collector dissipation	$T_f = 25^\circ\text{C}$ , per 1 chip	17.8	W
Tj	Junction temperature	(Note 1)	-20~+150	$^\circ\text{C}$

**Note 1** : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is  $150^\circ\text{C}$  (@  $T_f \leq 100^\circ\text{C}$ ). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to  $T_{j(\text{ave})} \leq 125^\circ\text{C}$  (@  $T_f \leq 100^\circ\text{C}$ ).

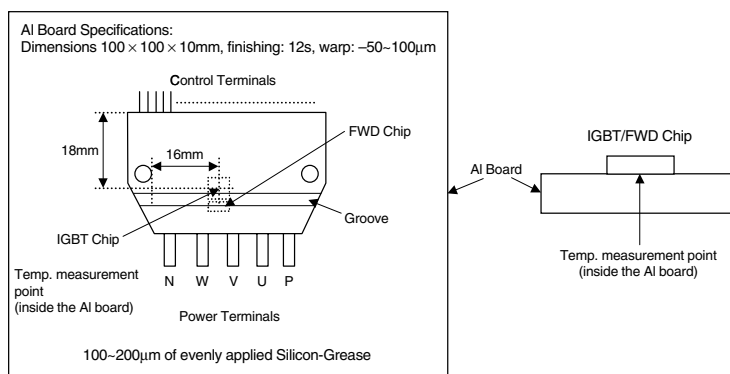
## CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
VD	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
VDB	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
VCIN	Input voltage	Applied between UP, VP, WP-VNC, UN, VN, WN-VNC	-0.5~VD+0.5	V
VFO	Fault output supply voltage	Applied between FO-VNC	-0.5~VD+0.5	V
IFO	Fault output current	Sink current at FO terminal	15	mA
VSC	Current sensing input voltage	Applied between CIN-VNC	-0.5~VD+0.5	V

## TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(Prot)	Self protection supply voltage limit (short-circuit protection capability)	VD = VDB = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$ , non-repetitive, less than 2 $\mu\text{s}$	330	V
Tf	Heat-fin operation temperature	(Note 2)	-20~+100	$^\circ\text{C}$
Tstg	Storage temperature		-40~+125	$^\circ\text{C}$
Viso	Isolation voltage	60Hz, Sinusoidal, 1 minute, connection pins to heat-sink plate	1500	Vrms

## Note 2 : Tf MEASUREMENT POINT



# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

## THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-f)Q}$	Junction-to-heat sink thermal resistance	Inverter IGBT part (per 1/6 module) (Note 3)	—	—	7.0	°C/W
$R_{th(j-f)F}$		Inverter FWD part (per 1/6 module) (Note 3)	—	—	8.0	°C/W

**Note 3 :** Grease with good thermal conductivity should be applied evenly about +100 $\mu$ m~+200 $\mu$ m on the contact surface of a DIP-IPM and a heat sink.

## ELECTRICAL CHARACTERISTICS ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

### INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{CIN} = 0\text{V}$	—	1.4	1.9	V
		$I_C = 3\text{A}$ , $T_j = 25^\circ\text{C}$ $I_C = 3\text{A}$ , $T_j = 125^\circ\text{C}$	—	1.5	2.05	
$V_{EC}$	FWD forward voltage	$T_j = 25^\circ\text{C}$ , $-I_C = 3\text{A}$ , $V_{CIN} = 5\text{V}$	—	1.9	2.6	V
$t_{on}$	Switching times	$V_{CC} = 280\text{V}$ , $V_D = V_{DB} = 15\text{V}$ $I_C = 3\text{A}$ , $T_j = 125^\circ\text{C}$ Inductive load (upper-lower arm) $V_{CIN} = 5 \leftrightarrow 0\text{V}$	0.4	0.9	1.35	$\mu\text{s}$
$t_{rr}$			—	0.25	—	$\mu\text{s}$
$t_{c(on)}$			—	0.35	0.60	$\mu\text{s}$
$t_{off}$			—	1.10	1.55	$\mu\text{s}$
$t_{c(off)}$			—	0.65	1.40	$\mu\text{s}$
$I_{CES}$			—	—	1	mA
	Collector-emitter cut-off current	$V_{CE} = V_{CES}$ $T_j = 125^\circ\text{C}$	—	—	10	

### CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$I_D$	Circuit current	$V_D = V_{DB} = 15\text{V}$ $V_{CIN} = 5\text{V}$	Total of $V_{P1-VNC}$ , $V_{N1-VNC}$		8.5	mA
			$V_{UFB-VUFS}$ , $V_{VFB-VVFS}$ , $V_{WFB-VWFS}$		1.0	
		$V_D = V_{DB} = 15\text{V}$ $V_{CIN} = 0\text{V}$	Total of $V_{P1-VNC}$ , $V_{N1-VNC}$		9.7	mA
			$V_{UFB-VUFS}$ , $V_{VFB-VVFS}$ , $V_{WFB-VWFS}$		1.0	
$V_{FOH}$	Fault output voltage	$V_{SC} = 0\text{V}$ , $F_O = 10\text{k}\Omega$ 5V pull-up	4.9	—	—	V
$V_{FOL}$		$V_{SC} = 1\text{V}$ , $I_{FO} = 1.5\text{mA}$	—	0.6	0.9	V
$V_{FOsat}$		$V_{SC} = 1\text{V}$ , $I_{FO} = 15\text{mA}$	0.8	1.2	1.8	V
$V_{SC(ref)}$	Short-circuit trip level	$T_j = 25^\circ\text{C}$ , $V_D = 15\text{V}$ (Note 4)	0.43	0.48	0.53	V
$UV_{DBt}$	Supply circuit under-voltage protection	$T_j \leq 125^\circ\text{C}$	Trip level		10.0	V
$UV_{DBr}$			Reset level		10.5	V
$UV_{Dt}$			Trip level		10.3	V
$UV_{Dr}$			Reset level		10.8	V
$t_{FO}$	Fault output pulse width	$C_{FO} = 22\text{nF}$ (Note 5)	1.0	1.8	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between:	0.8	1.4	2.0	V
$V_{th(off)}$	OFF threshold voltage	UP, VP, WP-VNC, UN, VN, WN-VNC	2.5	3.0	4.0	V

**Note 4 :** Short-circuit protection operates only at the low-arms. Please select the value of the external shunt resistor such that the SC trip level is less than 5.1A

**5 :** Fault signal is outputted when the low-arm short-circuit or control supply under-voltage protective functions operate. The fault output pulse-width  $t_{FO}$  depends on the capacitance value of  $C_{FO}$  according to the following approximate equation. :  $C_{FO} = (12.2 \times 10^{-6}) \times t_{FO} [\text{F}]$

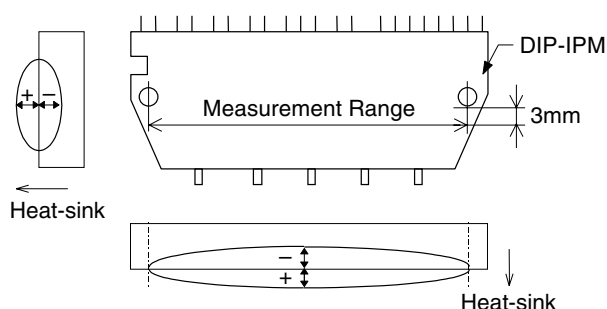
# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	—	0.59	0.78	0.98	N·m
Terminal pulling strength	Weight 9.8N	EIAJ-ED-4701	10	—	—	s
Bending strength	Weight 4.9N. 90deg bend	EIAJ-ED-4701	2	—	—	times
Weight		—	—	20	—	g
Heat-sink flatness	(Note 6)	—	-50	—	100	μm

### Note 6: Measurement point of heat-sink flatness



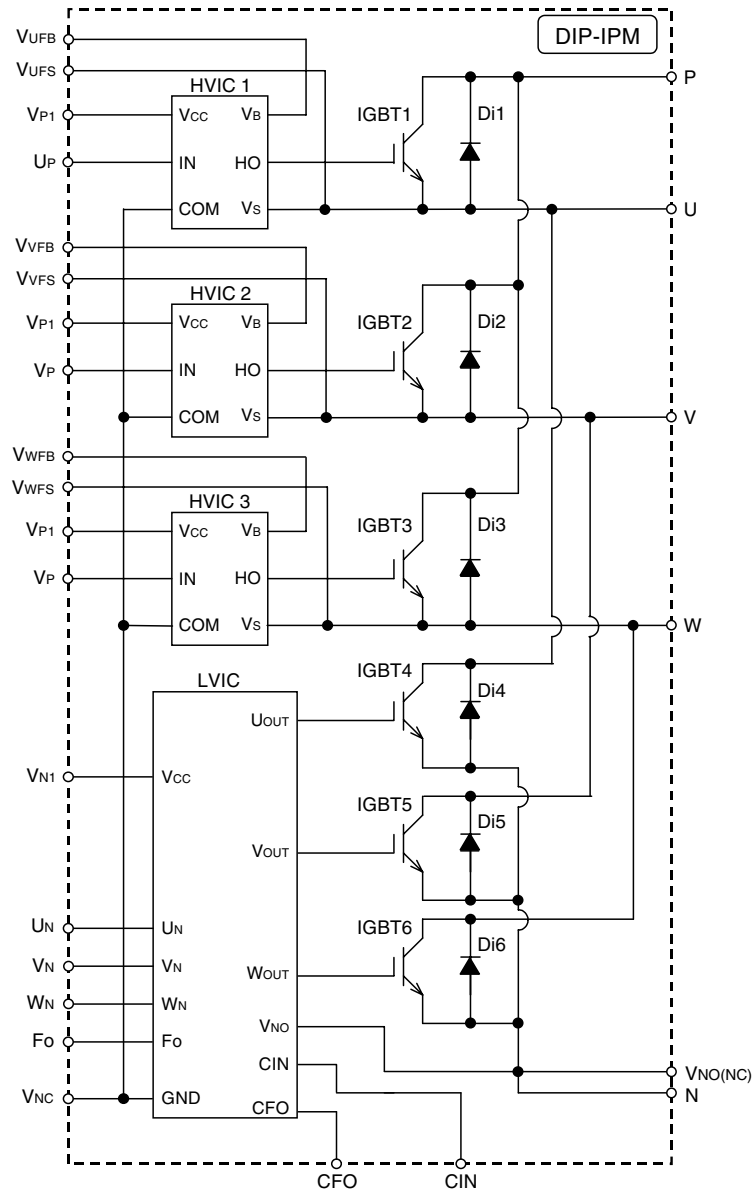
## RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage	Applied between P-N	0	280	330	V
V <sub>D</sub>	Control supply voltage	Applied between V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	13.5	15.0	16.5	V
V <sub>DB</sub>	Control supply voltage	Applied between V <sub>UFB</sub> -V <sub>UFS</sub> , V <sub>VFB</sub> -V <sub>VFS</sub> , V <sub>WFB</sub> -V <sub>WFS</sub>	13.5	15.0	16.5	V
ΔV <sub>D</sub> , ΔV <sub>DB</sub>	Control supply variation		-1	—	1	V/μs
t <sub>dead</sub>	Arm shoot-through blocking time	For each input signal	1.5	—	—	μs
f <sub>PWM</sub>	PWM input frequency	T <sub>J</sub> ≤ 125°C, T <sub>r</sub> ≤ 100°C	—	5	—	kHz
V <sub>CIN(ON)</sub>	Input ON voltage	Applied between U <sub>P</sub> , V <sub>P</sub> , W <sub>P</sub> -V <sub>NC</sub> , U <sub>N</sub> , V <sub>N</sub> , W <sub>N</sub> -V <sub>NC</sub>	0~0.65			V
V <sub>CIN(OFF)</sub>	Input OFF voltage		4.0~5.5			V

# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

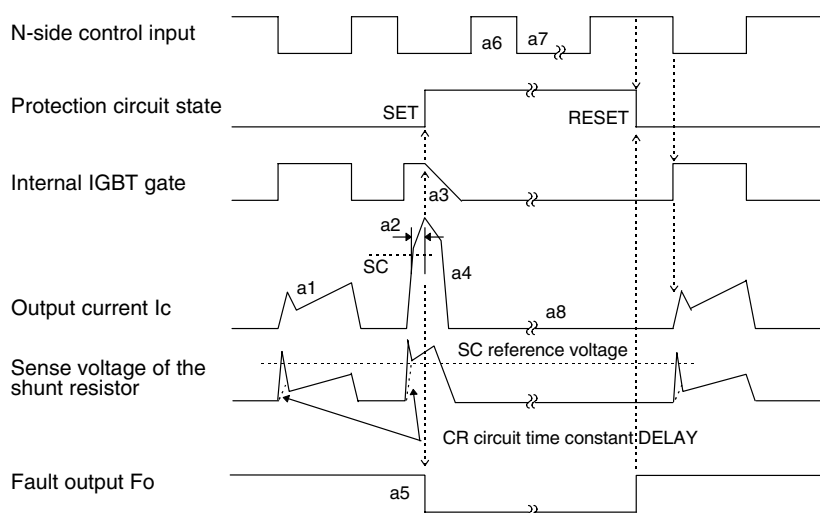


**Note:** The IGBTs gates and the HVICs COM terminals are connected to the dummy pins.

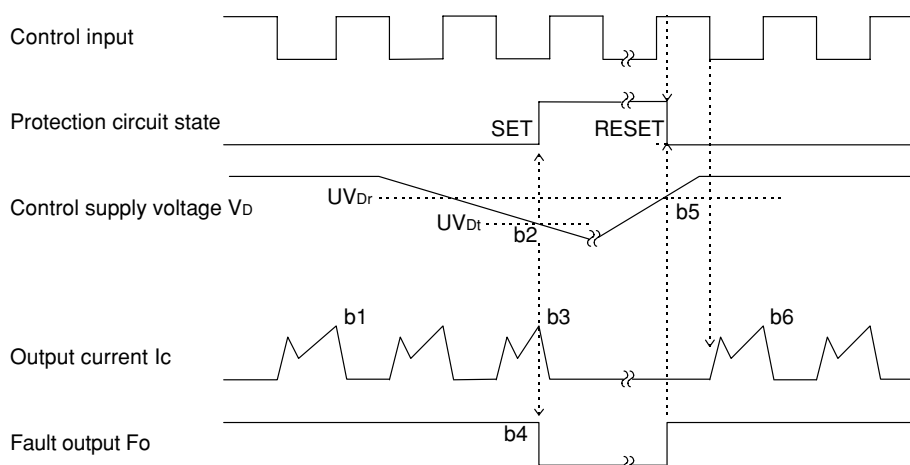
**Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS****[A] Short-Circuit Protection (N-side only)**

(For the external shunt resistor and CR connection, please refer to Fig. 3.)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short-circuit current detection (SC trigger).
- a3. IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. FO timer operation starts : The pulse width of the Fo signal is set by the external capacitor C<sub>FO</sub>.
- a6. Input "H" : IGBT OFF state.
- a7. Input "L" : IGBT ON state.
- a8. IGBT OFF state.

**[B] Under-Voltage Protection (N-side, UVd)**

- b1. Normal operation : IGBT ON and carrying current.
- b2. Under-voltage trip (UV<sub>Dt</sub>).
- b3. IGBT OFF in spite of control input condition.
- b4. FO timer operation starts.
- b5. Under-voltage reset (UV<sub>Dr</sub>).
- b6. Normal operation : IGBT ON and carrying current.



# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

## [C] Under-Voltage Protection (P-side, UVDB)

- c1. Control supply voltage rises : After the voltage level reaches UVDBr, the circuits start to operate when the next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under-voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input condition (there is no Fo signal output).
- c5. Under-voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.

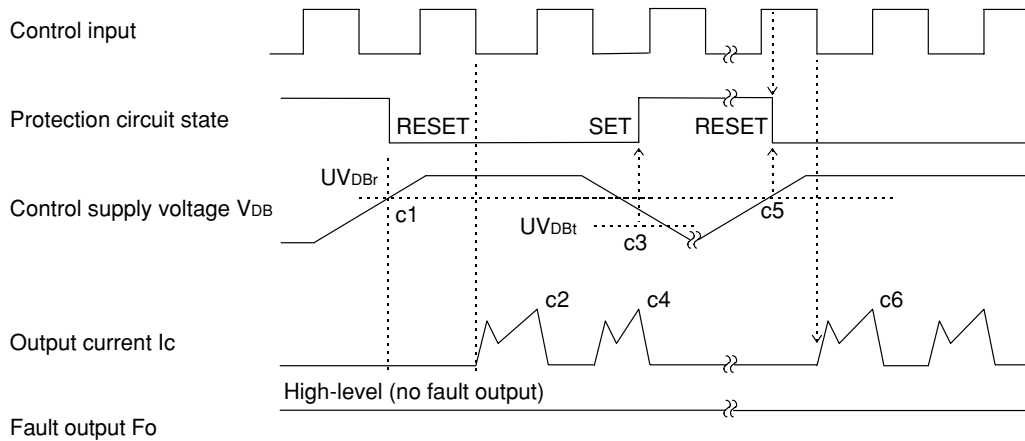
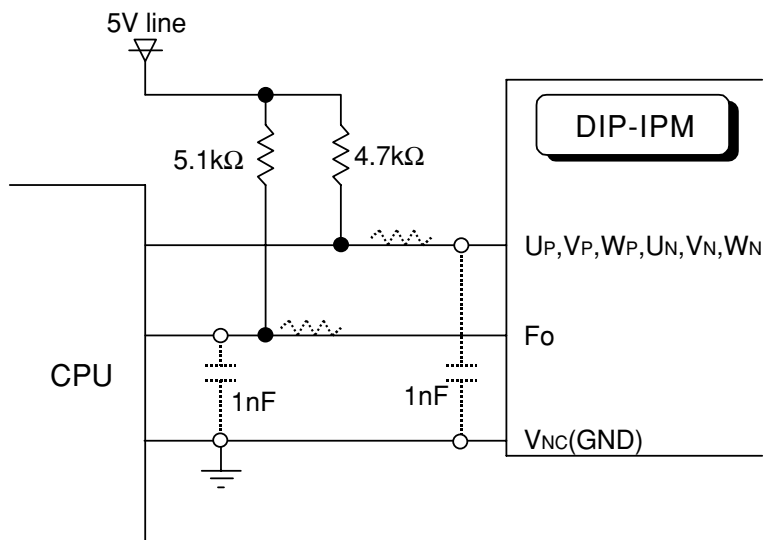


Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT



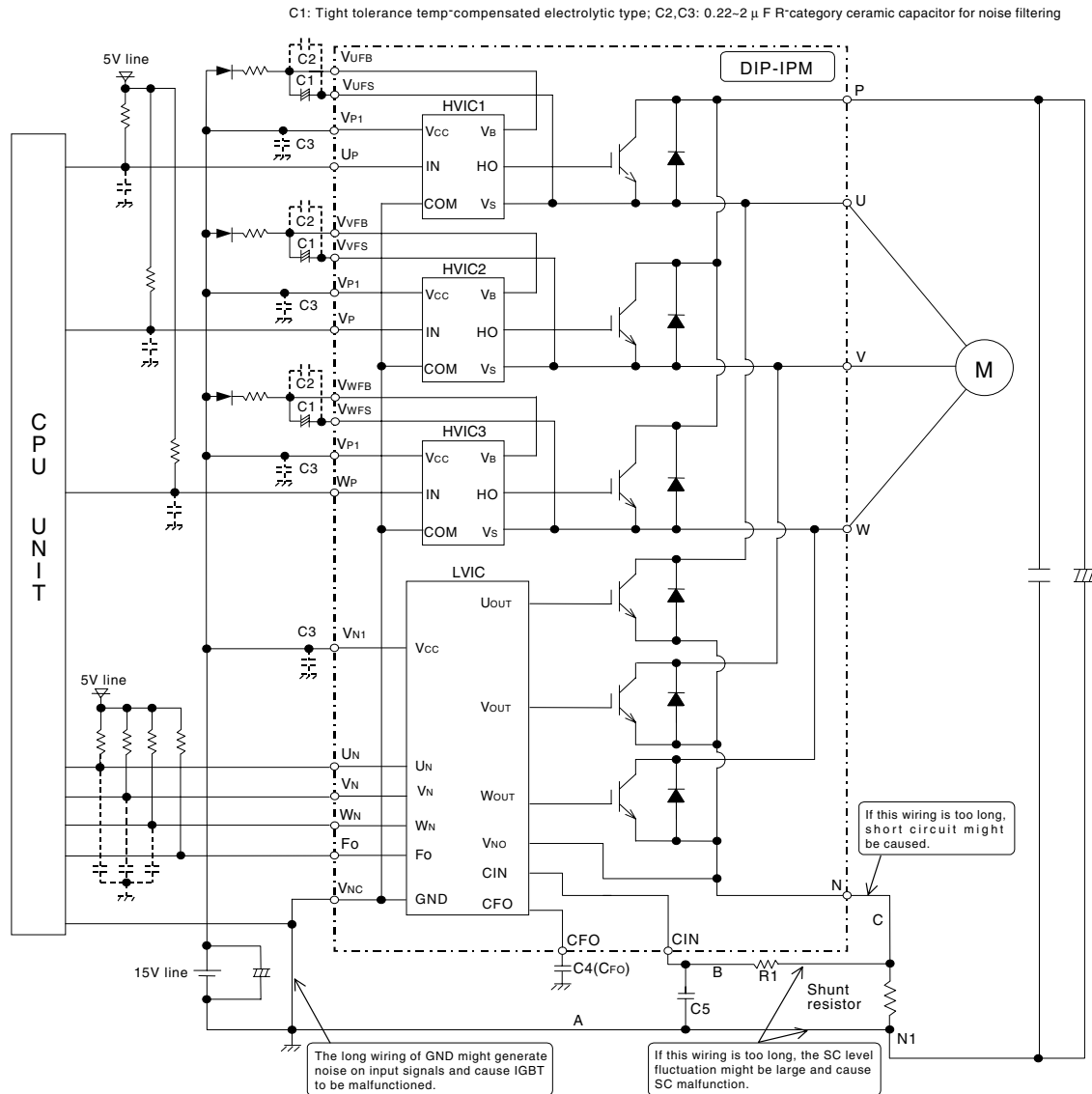
**Note :** RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedance of the application's printed circuit board.



# PS20341-N

TRANSFER-MOLD TYPE  
INSULATED TYPE

Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



**Note 1 :** To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible (less than 2cm).

**2 :** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

**3 :** Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1k $\Omega$  resistance.

**4 :** Fo output pulse width should be decided by connecting an external capacitor between Cfo and Vnc terminals (Cfo). (Example : Cfo = 22 nF  $\rightarrow$  tfo = 1.8 ms (typ.))

**5 :** Each input signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7k $\Omega$  resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2 $\mu$ F by-pass capacitor should be used across each power supply connection terminals.

**6 :** To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.

**7 :** In the recommended protection circuit, please select the R1Cs time constant in the range of 1.5~2 $\mu$ s.

**8 :** Each capacitor should be put as nearby the terminals of the DIP-IPM as possible.

**9 :** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 terminals should be as short as possible. Approximately a 0.1~0.22 $\mu$ F snubber capacitor between the P&N1 terminals is recommended.