

PM50CLA120

FLAT-BASE TYPE
INSULATED PACKAGE

PM50CLA120



FEATURE

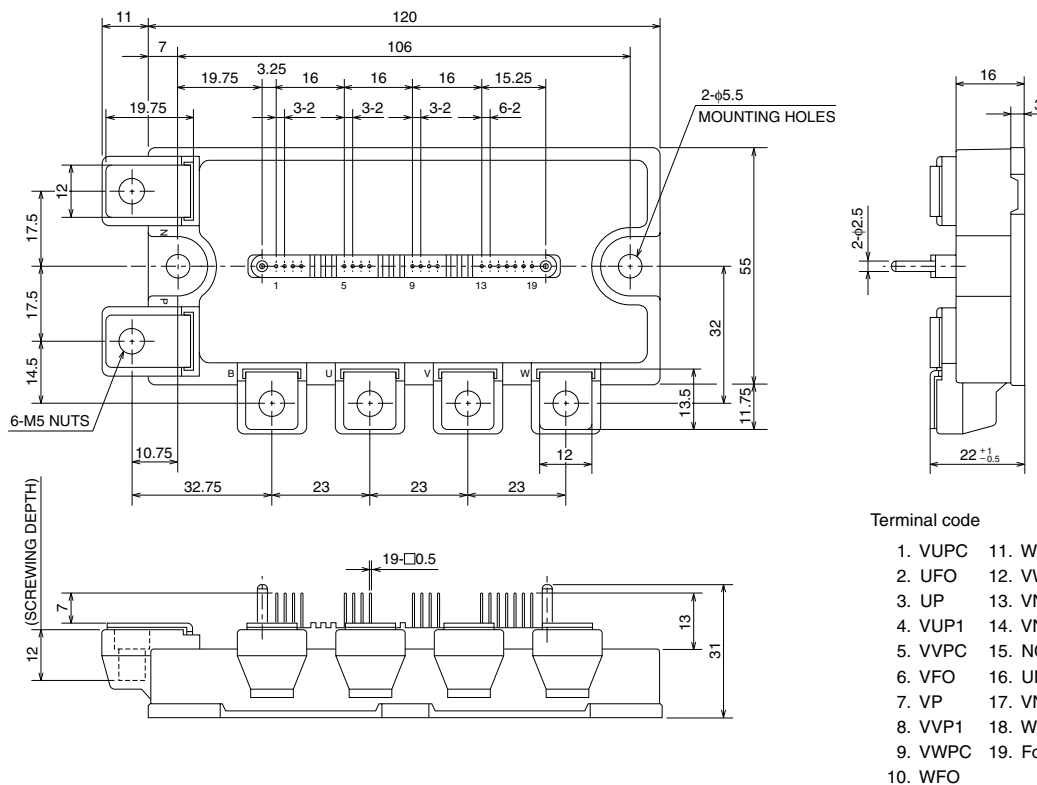
- a) Adopting new 5th generation IGBT (CSTBT) chip, which performance is improved by 1μm fine rule process.
For example, typical $V_{ce(sat)}=1.9V$ @ $T_j=125^{\circ}C$
- b) I adopt the over-temperature conservation by T_j detection of CSTBT chip, and error output is possible from all each conservation upper and lower arm of IPM.
- c) New small package
Reduce the package size by 10%, thickness by 22% from S-DASH series.
 - 3φ 50A, 1200V Current-sense IGBT type inverter
 - Monolithic gate drive & protection logic
 - Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
 - Acoustic noise-less 5.5kW/7.5kW class inverter application
 - UL Recognized Yellow Card No.E80276(N)
File No.E80271

APPLICATION

General purpose inverter, servo drives and other motor controls

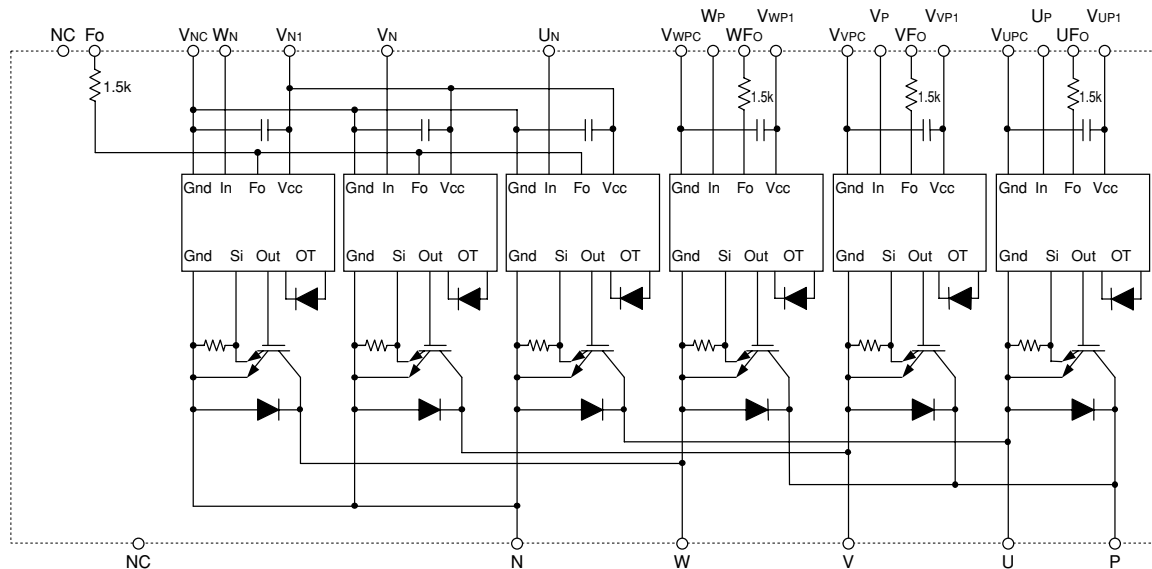
PACKAGE OUTLINES

Dimensions in mm



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INTERNAL FUNCTIONS BLOCK DIAGRAM**MAXIMUM RATINGS** (T_j = 25°C, unless otherwise noted)**INVERTER PART**

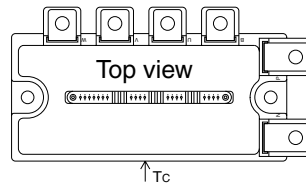
Symbol	Parameter	Condition	Ratings	Unit
V _{CES}	Collector-Emitter Voltage	V _D = 15V, V _{CIN} = 15V	1200	V
±I _C	Collector Current	T _C = 25°C	50	A
±I _{CP}	Collector Current (Peak)	T _C = 25°C	100	A
P _C	Collector Dissipation	T _C = 25°C (Note-1)	369	W
T _j	Junction Temperature		-20 ~ +150	°C

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Supply Voltage	Applied between : V _{UP1} -V _{UPC} V _{VPC} -V _{VPC} , V _{WP1} -V _{WPC} , V _{N1} -V _N	20	V
V _{CIN}	Input Voltage	Applied between : U _P -V _{UPC} , V _P -V _{VPC} W _P -V _{WPC} , U _N • V _N • W _N -V _N	20	V
V _{Fo}	Fault Output Supply Voltage	Applied between : U _{Fo} -V _{UPC} , V _{Fo} -V _{VPC} , W _{Fo} -V _{WPC} F _O -V _N	20	V
I _{Fo}	Fault Output Current	Sink current at U _{Fo} , V _{Fo} , W _{Fo} , F _O terminals	20	mA

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Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = +125°C Start	800	V
V _{CC(surge)}	Supply Voltage (Surge)	Applied between : P-N, Surge value	1000	V
T _c	Module Case Operating Temperature	(Note-1)	-20 ~ +100	°C
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

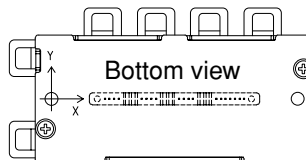
(Note-1) T_c (base plate) measurement point is below.**THERMAL RESISTANCES**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT (per 1 element) (Note-2)	—	—	0.26*	°C/W
R _{th(j-c)F}		Inverter FWDi (per 1 element) (Note-2)	—	—	0.39*	
R _{th(j-c)Q}		Inverter IGBT (per 1 element) (Note-1)	—	—	0.34	
R _{th(j-c)F}		Inverter FWDi (per 1 element) (Note-1)	—	—	0.51	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied (Note-2)	—	—	0.038	

* If you use this value, R_{th(f-a)} should be measured just under the chips.(Note-2) T_c (under the chip) measurement point is below.

(Unit : mm)

axis \ arm	UP		VP		WP		UN		VN		WN	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	28.3	28.4	65.0	64.9	87.0	86.9	39.3	39.2	54.0	54.1	76.0	76.1
Y	-7.7	1.5	-7.7	1.5	-7.7	1.5	5.7	-3.5	5.7	-3.5	5.7	-3.5

**ELECTRICAL CHARACTERISTICS** (T_j = 25°C, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A V _{CIN} = 0V (Fig. 1)	—	1.8	2.3	V
V _{EC}	FWDi Forward Voltage	-I _C = 50A, V _D = 15V, V _{CIN} = 15V (Fig. 2)	—	2.5	3.5	
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 600V, I _C = 50A T _j = 125°C Inductive Load (Fig. 3,4)	0.5	1.0	2.5	μs
t _{rr}			—	0.5	0.8	
t _{c(on)}			—	0.4	1.0	
t _{off}			—	2.0	3.0	
t _{c(off)}			—	0.7	1.2	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _{CIN} = 15V (Fig. 5)	—	—	1	mA
			—	—	10	

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Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Id	Circuit Current	V _D = 15V, V _{CIN} = 15V	—	15	25	mA
			—	5	10	
V _{th(ON)}	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC	1.2	1.5	1.8	V
V _{th(OFF)}	Input OFF Threshold Voltage		1.7	2.0	2.3	
SC	Short Circuit Trip Level	−20 ≤ T _j ≤ 125°C, V _D = 15V (Fig. 3,6)	100	—	—	A
t _{off(SC)}	Short Circuit Current Delay Time	V _D = 15V (Fig. 3,6)	—	0.2	—	μs
OT	Over Temperature Protection	V _D = 15V Detect T _j of IGBT chip	Trip level	135	145	°C
OT _r			Reset level	—	125	
UV	Supply Circuit Under-Voltage Protection	−20 ≤ T _j ≤ 125°C	Trip level	11.5	12.0	V
UV _r			Reset level	—	12.5	
I _{FO(H)}	Fault Output Current	V _D = 15V, V _{FO} = 15V (Note-3)	—	—	0.01	mA
I _{FO(L)}			—	10	15	
t _{FO}	Minimum Fault Output Pulse Width	V _D = 15V (Note-3)	1.0	1.8	—	ms

(Note-3) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	380	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 800	V
V _D	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC (Note-4)	15.0 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 9.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

(Note-4) With ripple satisfying the following conditions: dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

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PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

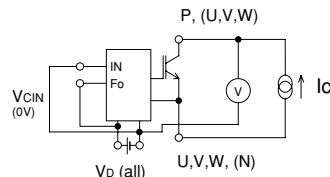


Fig. 1 $V_{CE(sat)}$ Test

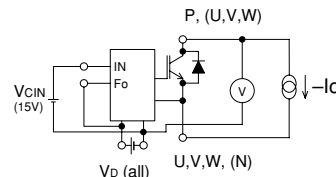
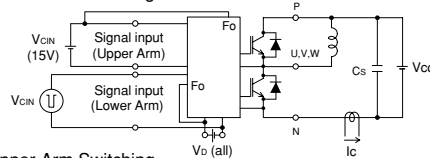


Fig. 2 V_{CE} Test

a) Lower Arm Switching



b) Upper Arm Switching

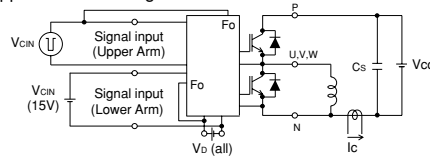


Fig. 3 Switching time and SC test circuit

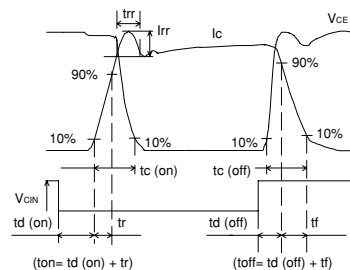


Fig. 4 Switching time test waveform

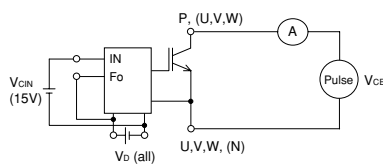


Fig. 5 I_{CES} Test

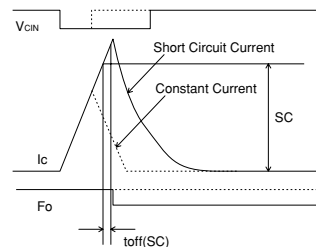
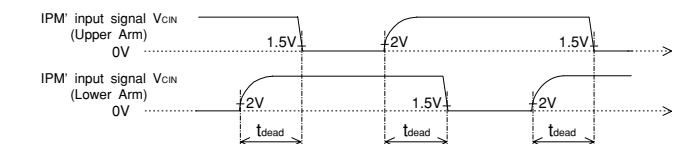


Fig. 6 SC test waveform



1.5V: Input on threshold voltage $V_{th(on)}$ typical value, 2V: Input off threshold voltage $V_{th(off)}$ typical value

Fig. 7 Dead time measurement point example

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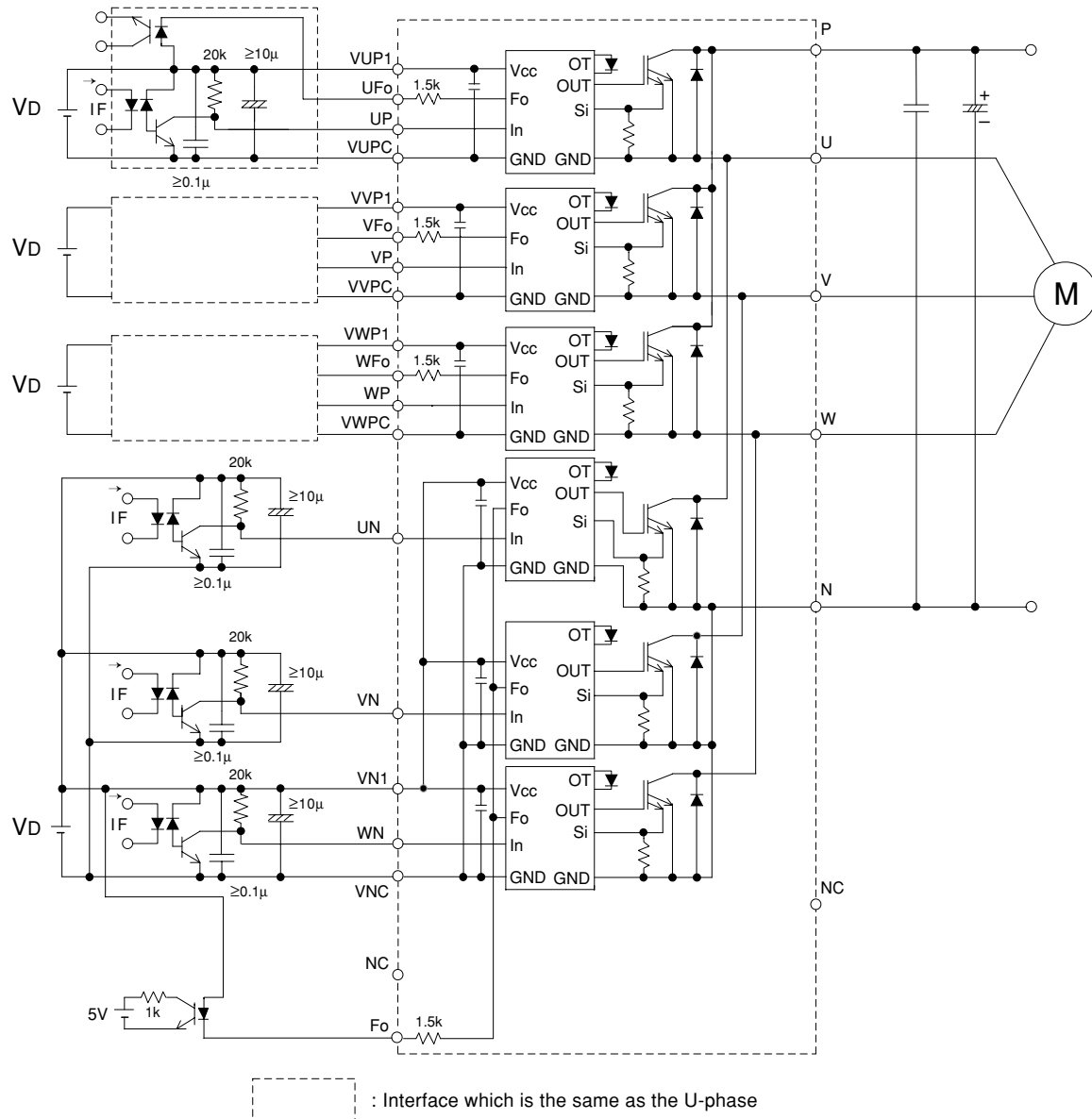


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: t_{PLH} , $t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.