

The documentation and process conversion measures necessary to comply with this document shall be completed by 27 May 2002.

INCH-POUND

MIL-PRF-19500/313F
 27 February 2002
 SUPERSEDING
 MIL-PRF-19500/313E
 18 August 2000

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, LOW POWER
 TYPES 2N2432, 2N2432A, 2N2432UB, JAN, JANTX, JANTXV, JANS, JANHC AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for low power, high speed chopper, NPN silicon transistors. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500. Two levels of product assurance are provided for die.

* 1.2 Physical dimensions. See figure 1 (T0-18), figures 2 and 3 (JANHC/JANKC die), and figure 4 (UB package).

* 1.3 Maximum ratings.

Type	P_T $T_A = +25^\circ\text{C}$	V_{CBO}	V_{CEO}	V_{ECO}	I_C	T_{STG}	T_J	$R_{\theta JA}$
	<u>mW</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>°C</u>	<u>°C</u>	<u>°C/mW</u>
2N2432	360 (1)	30	30	15	100	-65 to +200	-65 to +175	325
2N2432A	360 (1)	45	45	18	100	-65 to +200	-65 to +175	325
2N2432UB	360 (1)	30	30	15	100	-65 to +200	-65 to +175	325

(1) Derate linearly 2.06 mW/°C for $T_A > +25.5^\circ\text{C}$.

* 1.4 Primary electrical characteristics at $T_A = +25^\circ\text{C}$.

Limits	h_{FE1}	h_{FE2}	$h_{FE(inv)1}$		$V_{CE(sat)}$	$r_{ec(on)}$		$R_{\theta JC}$
	$V_{CE} = 5 \text{ V dc}$ $I_C = 10 \mu\text{A dc}$	$V_{CE} = 5 \text{ V dc}$ $I_C = 1 \text{ mA dc}$	$V_{CE} = 10 \text{ mA dc}$ $I_E = 200 \mu\text{A dc}$		$I_C = 10 \text{ mA dc}$ $I_B = 500 \mu\text{A dc}$	$I_e = 100 \mu\text{A ac (rms)}$ $I_B = 1 \text{ mA dc}, I_E = 0, f = 1 \text{ kHz}$		
			2N2432	2N2432A		2N2432 2N2432UB	2N2432A	
Min	30	80	2	3	<u>V dc</u>	<u>Ohms</u>	<u>Ohms</u>	<u>°C/mW</u>
Max		400			.15	20	15	.25

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

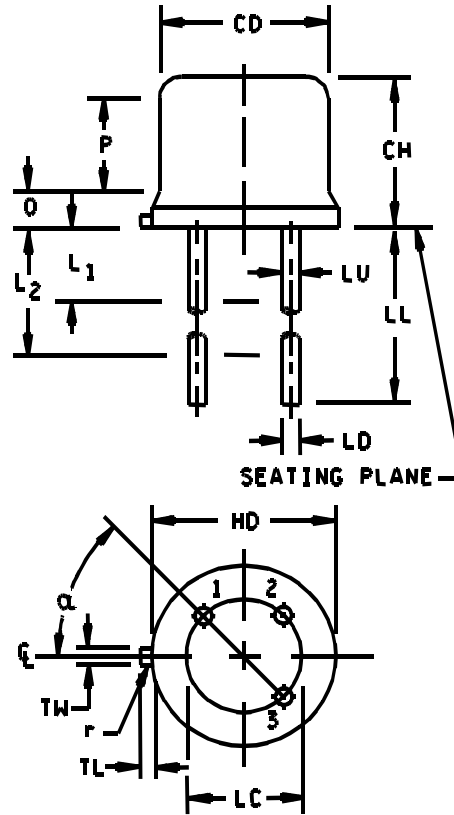
2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The requirements for acquiring the product described herein shall consist of this document and MIL-PRF-19500.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.4).

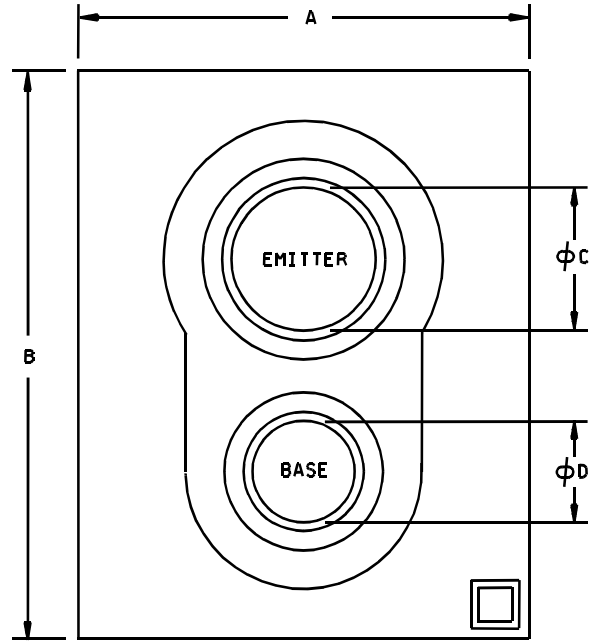
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L1		.050		1.27	7,8
L2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6



NOTES:

1. Dimension are in inches.
2. Metric equivalents are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ANSI Y14.5M, diameters are equivalent to ϕ x symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions (similar to TO-18).

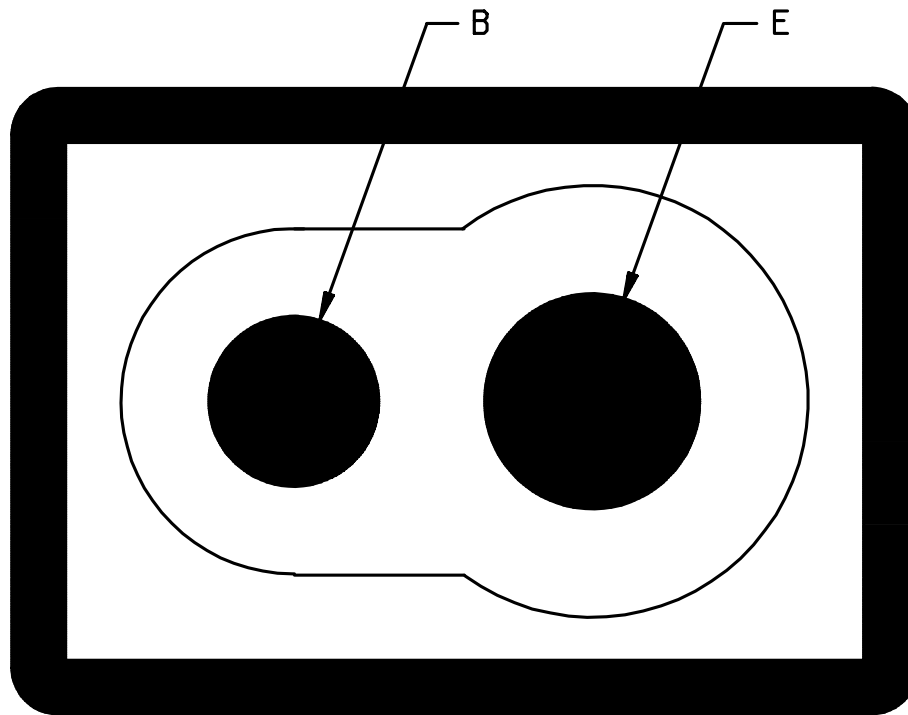


Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.013	.017	0.330	0.430
B	.017	.021	0.430	0.533
ϕC		.0048		0.122
ϕD		.0034		0.086

NOTES:

1. Chip thickness: .005 to .007 inch (0.127 to 0.178 millimeter).
2. Top metal: Aluminum 10,000 Å min, 12,000 Å nominal.
3. Back metal: Gold 2,000 Å min, 4,000 Å nominal.
4. Backside: Collector.

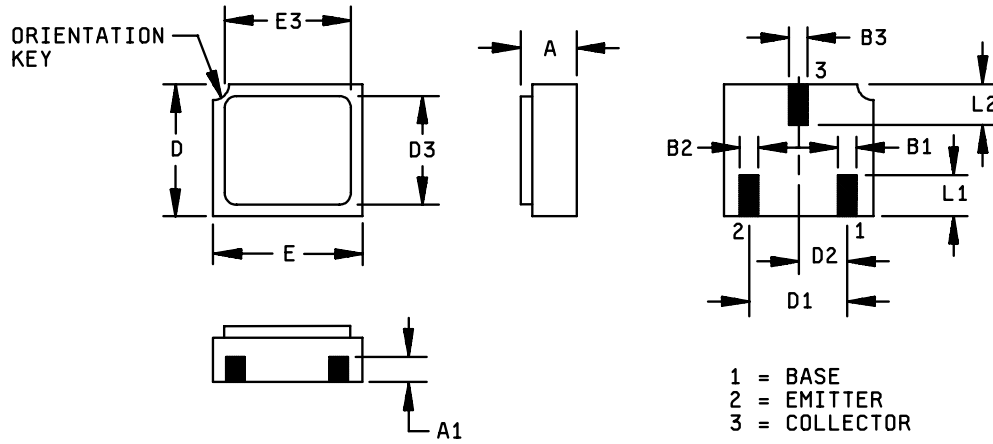
FIGURE 2. JANHC (A-version) die dimensions.



NOTES:

- | | |
|-------------------|---|
| 1. Chip size | .015 x .019 inch \pm .001 inch, (0.381 x 0.483 \pm 0.025 millimeter). |
| 2. Chip thickness | .010 \pm .0015 inch, (0.254 \pm 0.0038 millimeter). |
| 3. Top metal | Aluminum 15,000Å minimum, 18,000Å nominal. |
| 4. Back metal | A. Gold 2,500Å minimum, 3,000Å nominal.
B. Eutectic Mount - No Gold. |
| 5. Backside | Collector |
| 6. Bonding pad | B = .003 inch (0.076 millimeter).
E = .004 inch diameter (0.076 millimeter). |
| 7. Passivation | Si ₃ N ₄ (Silicon Nitride) 2 kÅ min, 2.2 kÅ nom. |

FIGURE 3. Physical dimensions, JANHCA and JANKCA (B - version) die.



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.046	.056	0.97	1.42
A1	.017	.035	0.43	0.89
B1	.016	.024	0.41	0.61
B2	.016	.024	0.41	0.61
B3	.016	.024	0.41	0.61
D	.085	.108	2.41	2.74
D1	.071	.079	1.81	2.01
D2	.035	.039	0.89	0.99
D3	.085	.108	2.41	2.74
E	.115	.128	2.82	3.25
E3		.128		3.25
L1	.022	.038	0.56	0.96
L2	.022	.038	0.56	0.96

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

* FIGURE 4. Physical dimensions, surface mount (UB version).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

$V_{(BR)ECO}$ - - - Breakdown voltage, emitter to collector, with base open circuited.

$h_{FE(inv)}$ - - - Forward current transfer ratio except that the collector and emitter shall be interchanged.

I_e - - - - Emitter current (rms).

$r_{ec(on)}$ - - - Small signal emitter to collector on state resistance.

V_{BC} - - - - Base to collector voltage.

$V_{EC(ofs)}$ - - - Emitter to collector offset voltage, i.e., open circuit voltage between emitter and collector when the base to collector junction is forward biased.

V_{ec} - - - - Emitter to collector voltage (rms).

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, and 4.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table 1.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4, and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC devices. JANHC and JANKC devices shall be qualified in accordance with MIL-PRF-19500.

MIL-PRF-19500/313F

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
*3c	Thermal impedance, method 3131 of MIL-STD-750.	Thermal impedance, method 3131 of MIL-STD-750.
9	I_{CBO2} , h_{FE1}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CBO2} ; h_{FE1} ; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE1} = ± 15 percent.	I_{CBO2} , h_{FE1}
12	See 4.3.1 240 hours minimum	See 4.3.1 80 hours minimum
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent.	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc; apply P_{TMAX} = 360 mW.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500 "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with group A, subgroup 2 and table III herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with group A, subgroup 2 and table III herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} = 10 \text{ V dc.}$
B5	1027	(Note: If a failure occurs, resubmission shall be at the test conditions of the original sample.) $V_{CB} = 10 \text{ V dc, } P_D \geq 100 \text{ percent of maximum rated } P_T \text{ (see 1.3).}$ Option 1: 96 hours minimum sample size in accordance with table VIa of MIL-PRF-19500, adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum. Option 2: 216 hours minimum, sample size = 45, $c = 0$; adjust T_A or P_D to achieve $T_J = +225^\circ\text{C}$ minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a group B failure, the manufacturer may pull a new sample at double size from either the failed assembly lot or from another assembly lot from the same wafer lot. If the new "assembly lot" option is exercised, the failed assembly lot shall be scrapped.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1039	Steady-state life: Test condition B, 1,000 hours, $V_{CB} = 10 - 30 \text{ V dc}$, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum power dissipation $P_D \geq 75 \text{ percent of maximum rated } P_T$ as defined in 1.3 herein.
2	1039	The steady-state life test of step 1 shall be extended to 1,000 hrs for each die design. Samples shall be selected from a wafer lot every twelve months of wafer production. Group B, step 2 shall not be required more than once for any single wafer lot. $n = 45, c = 0.$
3	1032	High-temperature life (non-operating), $t = 340 \text{ hours, } T_A = +200^\circ\text{C. } n = 22, c = 0.$

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Must be chosen from an inspection lot that has been submitted to and passed group A, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with group A, subgroup 2 and table III herein.

4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E.
C5	3131	See 4.5.7.
C6	1026	1,000 hours at $V_{CB} = 10$ to 30 V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum power dissipation $P_D \geq 75$ percent of maximum rated P_T as defined in 1.3 herein.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E.
C5	3131	See 4.5.7.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes group A tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be performed for qualification or re-qualification only. The tests specified in table II herein shall be performed to maintain qualification.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Emitter to collector cutoff current. Method of test shall be in accordance with method 3041 of MIL-STD-750, test condition C, except that all references to the collector and emitter of the transistor under test shall be interchanged.

4.5.3 Emitter to collector breakdown voltage. Method of test shall be in accordance with method 3011 of MIL-STD-750, test condition D, except that all references to the collector and emitter of the transistor under test shall be interchanged.

4.5.4 Forward current transfer ratio (inverted connection). Method of test shall be in accordance with method 3076 of MIL-STD-750, except that all references to the collector and emitter of the transistor under test shall be interchanged. Then $h_{FE(inv)} = I_E / I_B$.

4.5.5 Emitter to collector offset voltage. The transistor shall be tested in the circuit on figure 5. The base current shall be adjusted to the specified value. The voltage between the emitter and collector shall be measured using a voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement.

4.5.6 Small signal emitter to collector on-state resistance. The transistor shall be tested in the circuit of figure 6. The base current shall be adjusted to the specified value and an ac sinusoidal signal current, I_e , of the specified rms value shall be applied between the emitter and collector. The rms voltage V_{ec} , between the emitter and collector shall be measured using an ac voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement. The small signal emitter to collector on-state resistance shall then be determined as follows:

$$r_{ec(on)} = V_{ec} / I_E$$

Where V_{ec} is the rms voltage between the emitter and collector.

4.5.7 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750. The following details shall apply:

- a. Collector current magnitude during power application shall be 30 mA dc.
- b. Collector emitter voltage magnitude shall be 10 V dc.
- c. Reference temperature measuring point shall be the case.
- d. Reference point temperature shall be selected with $+25^{\circ}\text{C} \leq T_R \leq +75^{\circ}\text{C}$ and recorded before the test is started.
- e. Mounting arrangement shall be with heat sink to case.
- f. Maximum limit for $R_{\theta JC}$ shall be $0.25^{\circ}\text{C}/\text{mW}$.

MIL-PRF-19500/313F

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
*Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
*Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>4/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements <u>4/</u>		Group A, subgroup 2				
Bond strength <u>3/ 4/</u>	2037	Precondition T _A = +250°C at t = 24 hrs or T _A = +300°C at t = 2 hrs n = 11 wires, c = 0				
Decap internal visual design verification <u>4/</u>	2075	n = 4, c = 0.				
<u>Subgroup 2</u>						
*Breakdown voltage collector to emitter 2N2432, 2N2432UB 2N2432A	3011	Bias condition D; I _C = 10 mA dc; pulsed (see 4.5.1)	V _{(BR)CEO}	30 45		V dc V dc
*Collector to base cutoff current 2N2432, 2N2432UB 2N2432A	3036	Bias condition D V _{CB} = 30 V dc V _{CB} = 45 V dc	I _{CBO1}		100 100	μA dc μA dc
*Breakdown voltage emitter to collector 2N2432, 2N2432UB 2N2432A	3011	Bias condition D; I _E = 100 μA dc; I _E = 0 (see 4.5.3)	V _{(BR)ECO1}	15 18		V dc V dc
Breakdown voltage emitter to collector	3011	Bias condition D; I _E = 10 mA dc; I _B = 0; pulsed (see 4.5.1 and 4.5.3)	V _{(BR)EC02}	10		V dc
*Collector to base cutoff current 2N2432, 2N2432UB 2N2432A	3036	Bias condition D V _{CB} = 25 V dc V _{CB} = 40 V dc	I _{CBO2}		10 10	nA dc nA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
*Collector to emitter cutoff current	3041	Bias condition C	I_{CES1}			
2N2432, 2N2432UB		$V_{CB} = 25 \text{ V dc}$			10	nA dc
2N2432A		$V_{CB} = 40 \text{ V dc}$			10	nA dc
Emitter to collector cutoff current	3041	Bias condition C; $V_{EC} = 15 \text{ V dc}$; $V_{BC} = 0$; (see 4.5.2)	I_{ECS1}		2	nA dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 15 \text{ V dc}$	I_{EBO}		2	nA dc
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}$; $I_C = 10 \mu\text{A dc}$	h_{FE1}	30		
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}$; $I_C = 1 \text{ mA dc}$	h_{FE2}	80	400	
*Forward-current transfer ratio (inverted connection)	3076	$V_{CE} = 5 \text{ V dc}$; $I_C = 0.2 \text{ mA dc}$; (see 4.5.4)	$h_{FE(inv)1}$			
2N2432, 2N2432UB				2		
2N2432A				3		
Saturation voltage and resistance	3071	$I_C = 10 \text{ V dc}$; $I_B = 0.5 \text{ mA dc}$	$V_{CE(sat)}$		0.15	V dc
*Emitter to collector offset voltage		$I_B = 200 \mu\text{A dc}$; $I_E = 0 \text{ mA dc}$ (see 4.5.5 and figure 6)	$V_{EC(ofs)1}$			
2N2432, 2N2432UB					0.5	mV dc
2N2432A					0.4	mV dc
*Emitter to collector offset voltage		$I_B = 1 \text{ mA dc}$; $I_E = 0 \text{ mA dc}$ (see 4.5.5 and figure 6)	$V_{EC(ofs)2}$			
2N2432, 2N2432UB					1.0	mV dc
2N2432A					0.7	mV dc
<u>Subgroup 3</u>						
High-temperature operation:						
		$T_A = +125^\circ\text{C}$				
*Collector to emitter cutoff current	3041	Bias condition C	I_{CES2}			
2N2432, 2N2432UB		$V_{CB} = 25 \text{ V dc}$			250	nA dc
2N2432A		$V_{CB} = 40 \text{ V dc}$			250	nA dc
Emitter to collector cutoff current	3041	Bias condition C; $V_{EC} = 15 \text{ V dc}$; $V_{BC} = 0$ (see 4.5.2)	I_{ECS2}		200	nA dc
Low-temperature operation:						
		$T_A = -55^\circ\text{C}$				

See footnotes at end of table.

MIL-PRF-19500/313F

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}; I_C = 10 \text{ } \mu\text{A dc};$ pulsed (see 4.5.1)	h_{FE3}	10		
Forward-current transfer ratio	3076	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE4}	25		
Forward-current transfer ratio (inverted connection)	3076	$V_{CE} = 5 \text{ V dc}; I_E = 200 \text{ } \mu\text{A dc};$ pulsed (see 4.5.1 and 4.5.4)	$h_{FE(inv)2}$	1.8		
<u>Subgroup 4</u>						
*Small signal emitter collector on state resistance		$I_B = 1 \text{ mA dc}; I_E = 0;$ $I_e = 100 \text{ } \mu\text{A ac (rms)}; f = 1 \text{ kHz}$ (see 4.5.6 and figure 6)	$r_{ec(on)}$			
2N2432, 2N2432UB 2N2432A					20 15	Ω Ω
Small-signal short-circuit forward- current transfer ratio	3306	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ mA dc};$ $f = 20 \text{ MHz}$	$ h_{fe} $	2	10	
Open circuit output capacitance	3236	$V_{CB} = 0; I_E = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		12.0	pF
Input capacitance	3240	$V_{EB} = 0 \text{ V dc}; I_C = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{ibo}		12.0	pF
<u>Subgroups 5 and 6</u>						
Not applicable						
<u>Subgroup 7</u> <u>4/</u>						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup A1, double the sample size of the failed test or sequence of tests. A failure in group A, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

MIL-PRF-19500/313F

TABLE II. Group E inspection (all quality levels) - for qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See group A, subgroup 2 and table III herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	$V_{CB} = 10$ V dc, 6,000 cycles, forced air cooling allowed on cooling cycle only.	
Electrical measurements		See group A, subgroup 2 and table III herein.	
<u>Subgroup 3</u>			
Not applicable			
<u>Subgroup 4</u>			
Thermal resistance	3131	$R_{\theta JC}$ see 4.5.7.	22 devices c = 0
<u>Subgroup 5, 6, and 7</u>			
Not applicable			
<u>*Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V dc. Condition B for devices < 400 V dc.	

TABLE III. Groups B and C delta measurements. 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current 2N2432, 2N2432UB 2N2432A	3036	Bias condition D $V_{CB} = 25 \text{ V dc}$ $V_{CB} = 40 \text{ V dc}$	ΔI_{CB02}	100 percent of initial value or 5 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc};$ $I_C = 1.0 \text{ mA dc};$ pulsed see 4.5.1	Δh_{FE2}	± 25 percent change from initial reading.	

- 1/ Devices which exceed the group A limits for this test shall not be accepted.
- 2/ The delta measurements for group B, table VIa (JANS) of MIL-PRF-19500 are as follows: Subgroup 3, 5, and 6; see table III herein, steps 1 and 2.
- 3/ The delta measurements for 4.4.2.2 herein (group B, JAN, JANTX, and JANTXV) are as follows: Steps 1 and 2 of table III shall be performed after each step in 4.4.2.2 herein.
- 4/ The delta measurements for group C, table VII of MIL-PRF-19500 are as follows: Subgroup 6, see table III herein, steps 1 and 2 for JANS only.

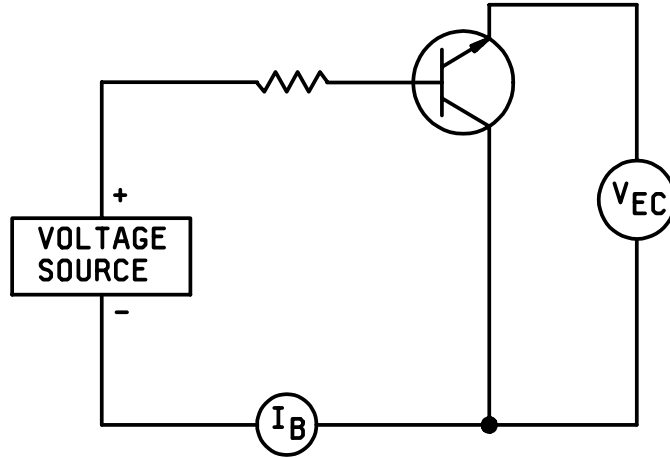


FIGURE 5. Emitter to collector offset voltage test circuit.

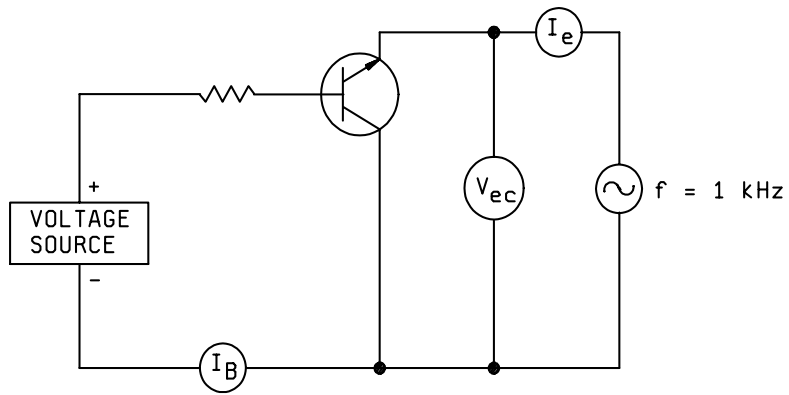


FIGURE 6. Small-signal emitter-collector on-state resistance test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- a. Title, number, and date of this specification.
- b. Issue of DoDISS to be cited in the solicitation and, if required, the specific issue of individual documents referenced (see 2.2).
- c. Lead finish (see 3.4.1).
- d. Type designation and product assurance level.
- e. Packaging requirements (see 5.1).

6.3 Suppliers of JANHC die. The qualified JANC suppliers with the applicable letter version (example, JANHCA2N2432 or JANHCA2N2432A) will be identified on the QML.

JANC ordering information		
PIN	Manufacturer	
	12498	43611
2N2432 2N2432A	JANHCA2N2432 JANHCA2N2432A	JANHCB2N2432 JANHCB2N2432A
2N2432 2N2432A		JANKCB2N2432 JANKCB2N2432A

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC-VQE, P.O. Box 3990, Columbus, OH 43216-5000.

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-4515-01)

Review activities:
Army - MI
Navy - AS, MC
Air Force - 19

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INSTRUCTIONS

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I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-PRF-19500/313F	2. DOCUMENT DATE 27 February 2002
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3. **DOCUMENT TITLE** SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, LOW POWER TYPES 2N2432, 2N2432A, 2N2432UB, JAN, JANTX, JANTXV, JANS, JANHC AND JANKC.

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) COMMERCIAL DSN FAX EMAIL	7. DATE SUBMITTED

8. PREPARING ACTIVITY

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c. ADDRESS Defense Supply Center Columbus ATTN: DSCC-VAC P.O. Box 3990 Columbus, OH 43216-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Standardization Program Office (DLSC-LM) 8725 John J. Kingman, Suite 2533 Fort Belvoir, VA 22060-6221 Telephone (703) 767-6888 DSN 427-6888