

MegaMOS™ FET

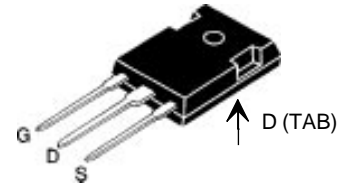
	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXTH/IXTM 67 N10	100 V	67 A	25 mΩ
IXTH/IXTM 75 N10	100 V	75 A	20 mΩ

N-Channel Enhancement Mode

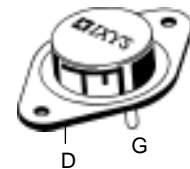


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	100	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	100	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	67N10	67 A
		75N10	75 A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	67N10	268 A
		75N10	300 A
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
M_d	Mounting torque	1.13/10 Nm/lb.in.	
Weight		TO-204 = 18 g, TO-247 = 6 g	
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	$^\circ\text{C}$

TO-247 AD (IXTH)



TO-204 AE (IXTM)



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard packages
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Low package inductance (< 5 nH)
 - easy to drive and to protect
- Fast switching times

Applications

- Switch-mode and resonant-mode power supplies
- Motor controls
- Uninterruptible Power Supplies (UPS)
- DC choppers

Advantages

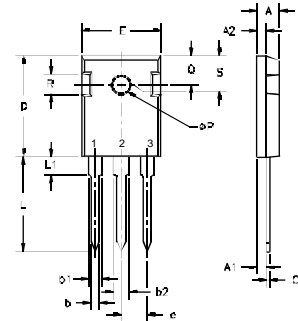
- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	100		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		V
I_{GSS}	$V_{GS} = \pm 20\text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100\text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		200 μA
		$T_J = 125^\circ\text{C}$		1 mA
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 0.5\ I_{D25}$ Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$	67N10		0.025 Ω
		75N10		0.020 Ω

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)			
		min.	typ.	max.	
g_{fs}	$V_{DS} = 10\text{ V}; I_D = 0.5 I_{D25}$, pulse test	25	30	S	
C_{iss} C_{oss} C_{rss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		4500	pF	
			1300	pF	
			550	pF	
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$ $R_G = 2\ \Omega$, (External)		40	60	ns
			60	110	ns
			100	140	ns
			30	60	ns
$Q_{g(on)}$ Q_{gs} Q_{gd}	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$		180	260	nC
			30	70	nC
			90	160	nC
R_{thJC} R_{thCK}			0.42	K/W	
		0.25		K/W	

Source-Drain Diode		Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
Symbol	Test Conditions	min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$	67N10 75N10		67 A 75 A
I_{SM}	Repetitive; pulse width limited by T_{JM}	67N10 75N10		268 A 300 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.75 V
t_{rr}	$I_F = I_S, -di/dt = 100\text{ A}/\mu\text{s}, V_R = 100\text{ V}$		300	ns

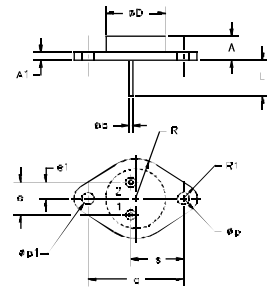
TO-247 AD (IXTH) Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L ₁		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	.242	BSC

TO-204AE (IXTM) Outline



Pins 1 - Gate 2 - Source
Case - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	6.4	11.4	.250	.450
A ₁	1.53	3.42	.060	.135
Øb	1.45	1.60	.057	.063
ØD		22.22		.875
e	10.67	11.17	.420	.440
e ₁	5.21	5.71	.205	.225
L	11.18	12.19	.440	.480
Øp	3.84	4.19	.151	.165
Øp ₁	3.84	4.19	.151	.165
q		30.15 BSC		1.187 BSC
R	12.58	13.33	.495	.525
R ₁	3.33	4.77	.131	.188
s	16.64	17.14	.655	.675

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Fig.1 Output Characteristics

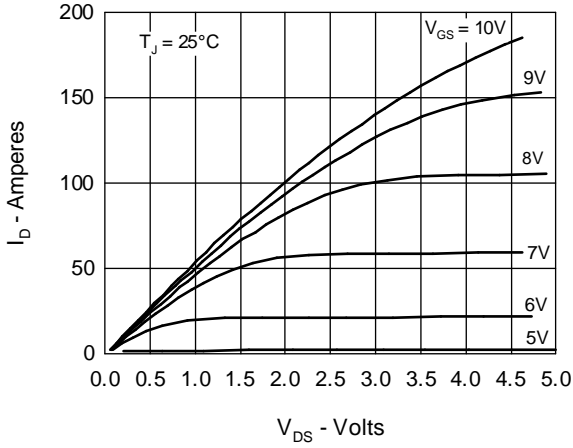


Fig.2 Input Admittance

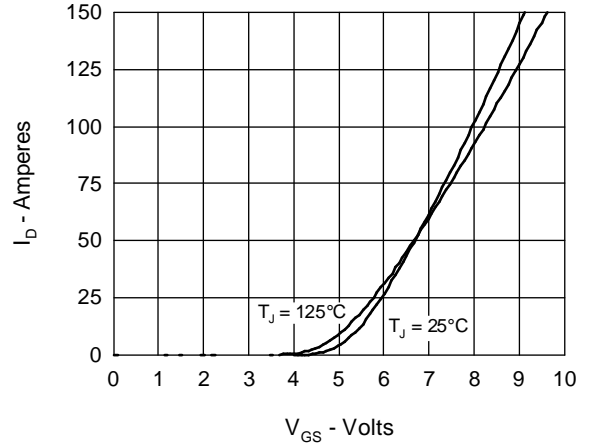


Fig.3 $R_{DS(on)}$ vs. Drain Current

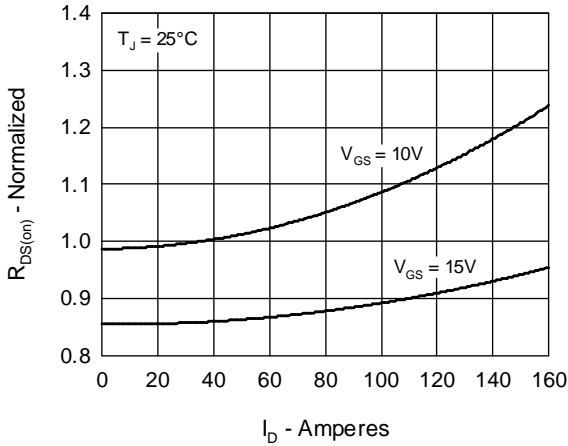


Fig.4 Temperature Dependence of Drain to Source Resistance

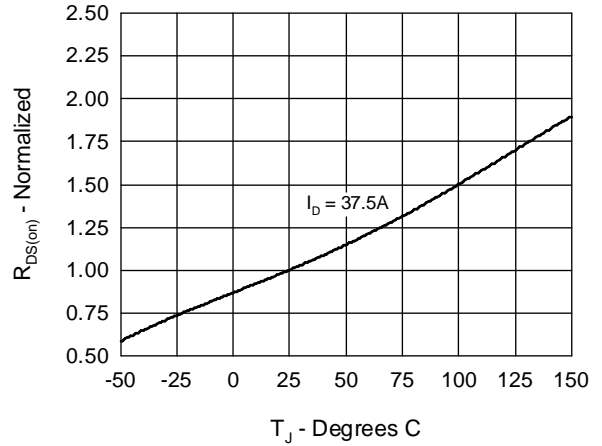


Fig.5 Drain Current vs. Case Temperature

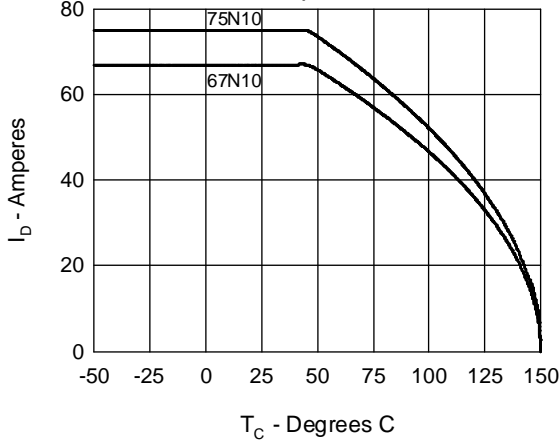


Fig.6 Temperature Dependence of Breakdown and Threshold Voltage

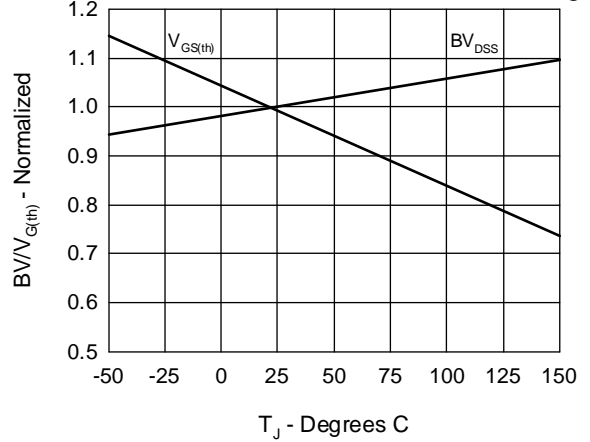


Fig.7 Gate Charge Characteristic Curve

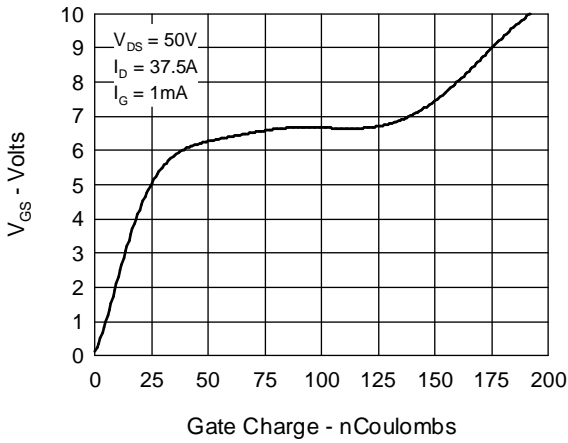


Fig.8 Forward Bias Safe Operating Area

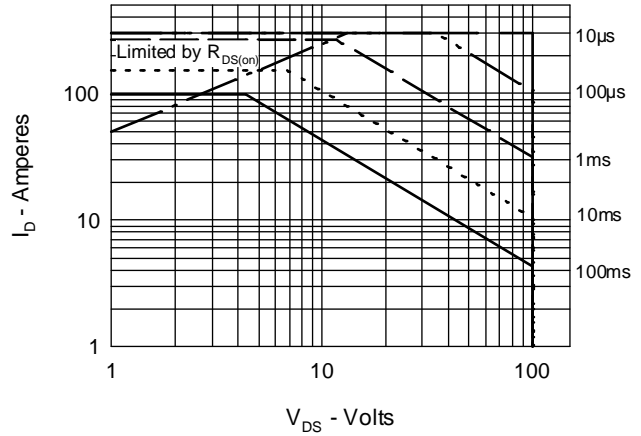


Fig.9 Capacitance Curves

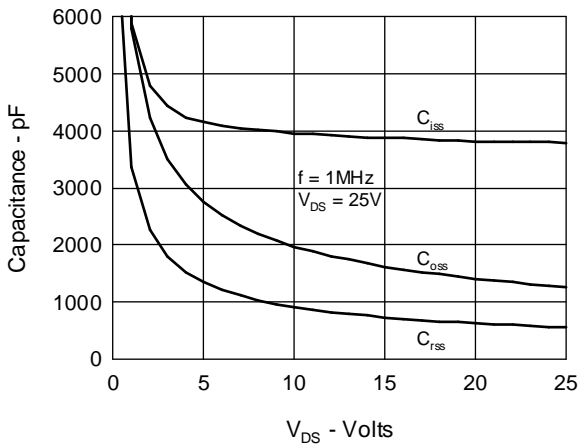


Fig.10 Source Current vs. Source to Drain Voltage

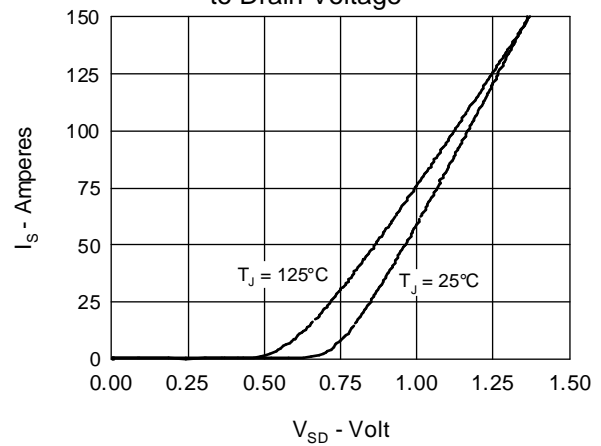


Fig.11 Transient Thermal Impedance

