File Number **2168**

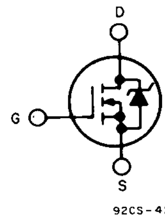
IRF634, IRF635, IRF636, IRF637

Avalanche Energy Rated N-Channel Power MOSFETs

N-CHANNEL ENHANCEMENT MODE

8.1A, and 6.5A, 275, 250V
r_{DS} (on) = 0.45Ω, 0.68Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *275, 250V rating - 120V AC line system operation*

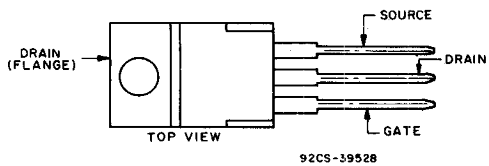


TERMINAL DIAGRAM

The IRF634, IRF635, IRF636, and IRF637 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

All types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



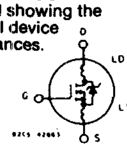
JEDEC TO-220AB

Absolute Maximum Ratings

Parameter		IRF634	IRF635	IRF636	IRF637	Units
V_{DS}	Drain - Source Voltage ①	250	250	275	275	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	250	250	275	275	V
I_D @ T_C = 25°C	Continuous Drain Current	8.1	6.5	8.1	6.5	A
I_D @ T_C = 100°C	Continuous Drain Current	5.1	4.1	5.1	4.1	A
I_{DM}	Pulsed Drain Current ③	32	26	32	26	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75				W
	Linear Derating Factor	0.6				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	180				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 [0.063 in. (1.6mm) from case for 10s]				°C

IRF634, IRF635
IRF636, IRF637

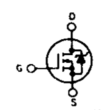
Electrical Characteristics @ T_C = 25° C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF636 IRF637	275	—	—	V	V_{GS} = 0V
		IRF634 IRF635	250	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF634 IRF636	8.1	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, V_{GS} = 10V
		IRF635 IRF637	6.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF634 IRF636	—	0.32	0.45	Ω	V_{GS} = 10V, I_D = 4.1A
		IRF635 IRF637	—	0.48	0.68	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.9	4.3	—	S(Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 4.1
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	180	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	52	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	9.1	14	ns	V_{DD} = 90V, I_D = 5.0A, Z_O = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	23	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	31	47	ns	
t_f	Fall Time	ALL	—	19	29	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	24	35	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.1	7.7	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	12	18	nC	
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

		Type	Min.	Typ.	Max.	Units	Test Conditions
$R_{th}JC$	Junction-to-Case	ALL	—	—	1.67	°C/W	
$R_{th}CS$	Case-to-Sink	ALL	—	0.5	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{th}JA$	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRF634 IRF636	—	—	8.1	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF635 IRF637	—	—	6.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF634 IRF636	—	—	32	A	
		IRF635 IRF637	—	—	26	A	
V_{SD}	Diode Forward Voltage ②	ALL	—	—	2.0	V	T_C = 25°C, I_S = 8.1A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	92	180	390	ns	T_J = 150°C, I_F = 8.1A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	0.63	1.3	2.7	μC	T_J = 150°C, I_F = 8.1A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_j = 25°C, L = 4.5MH, R_{gs} = 25Ω, I_{peak} = 8.1A. See figures 14, 15.

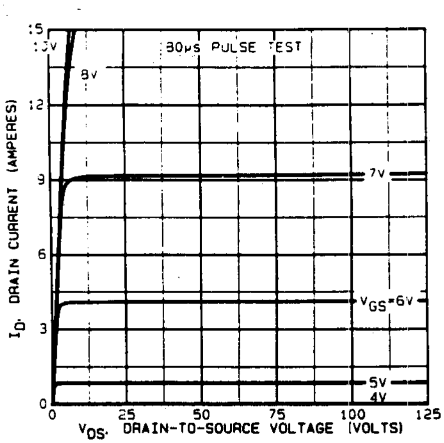


Fig. 1 — Typical Output Characteristics

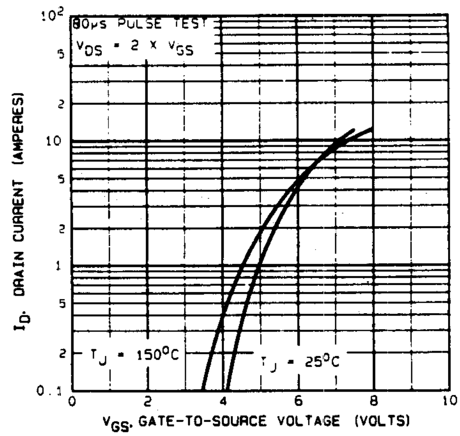


Fig. 2 — Typical Transfer Characteristics

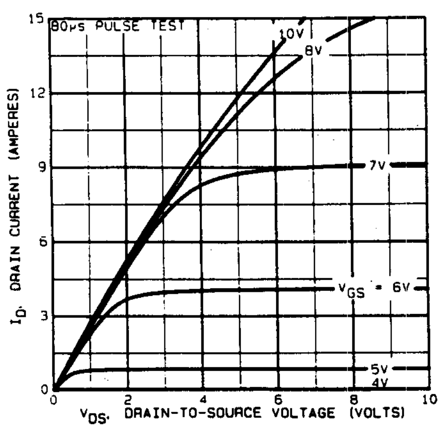


Fig. 3 — Typical Saturation Characteristics

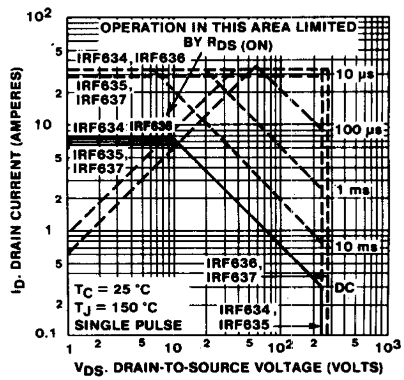


Fig. 4 — Maximum Safe Operating Area

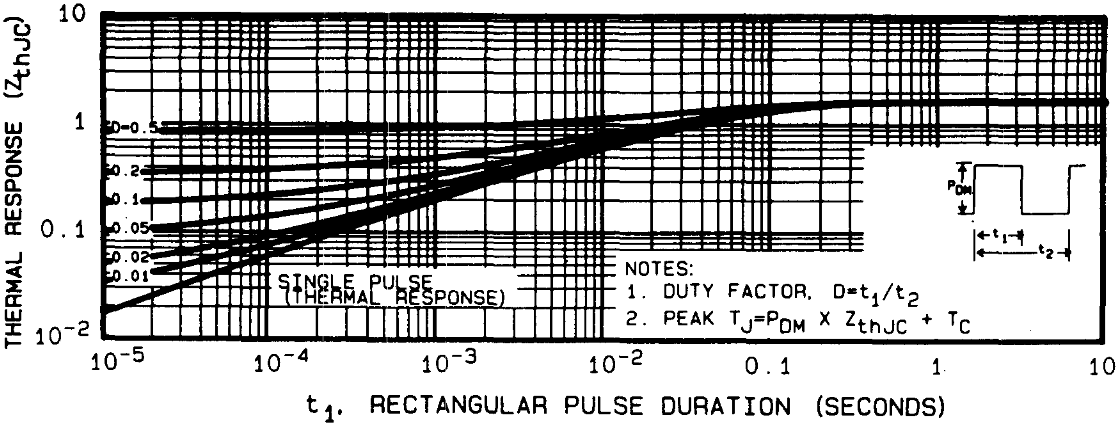


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

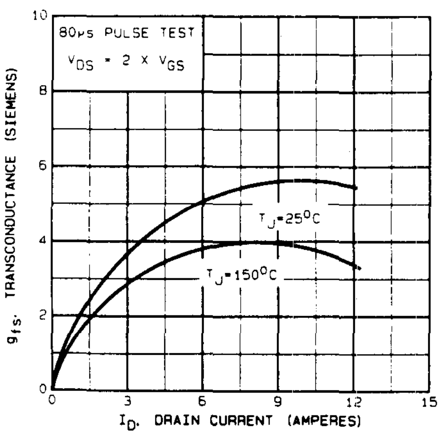


Fig. 6 — Typical Transconductance Vs. Drain Current

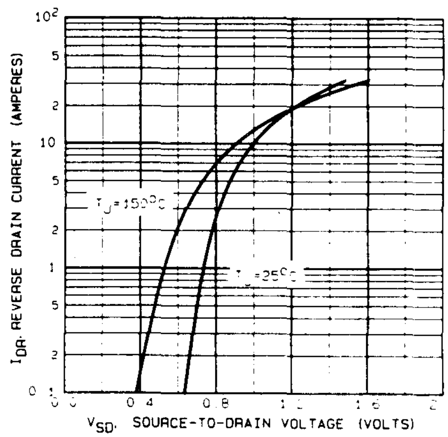


Fig. 7 — Typical Source-Drain Diode Forward Voltage

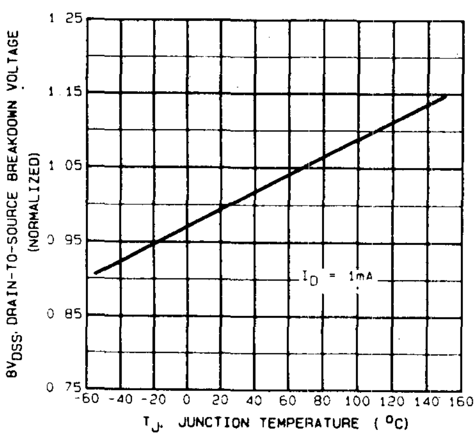


Fig. 8 — Breakdown Voltage Vs. Temperature

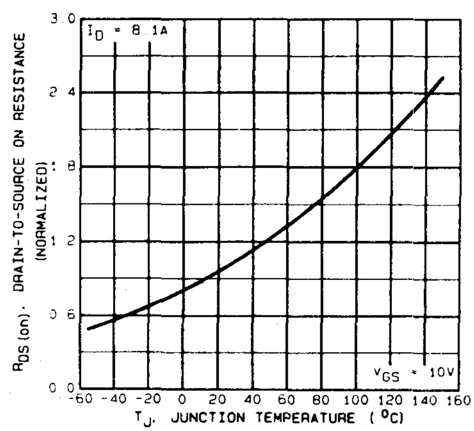


Fig. 9 — Normalized On-Resistance Vs. Temperature

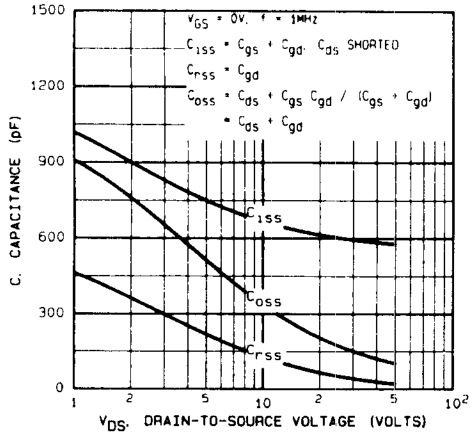


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

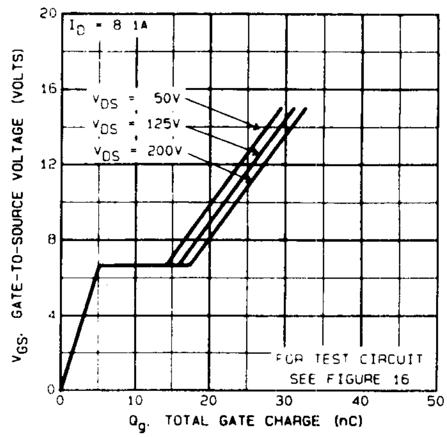


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

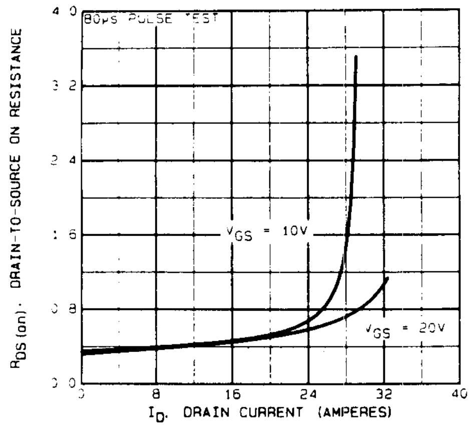


Fig. 12 — Typical On-Resistance Vs. Drain Current

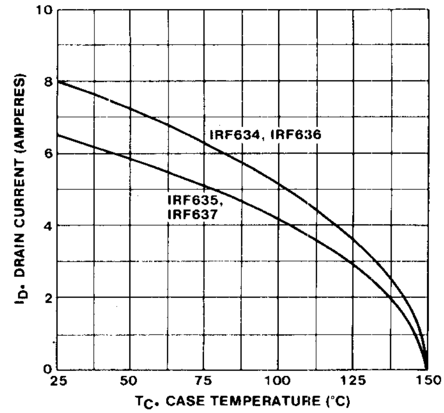


Fig. 13 — Maximum Drain Current Vs. Case Temperature

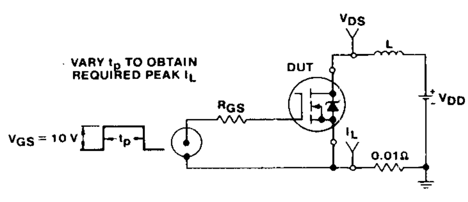


Fig. 14 — Unclamped Energy Test Circuit

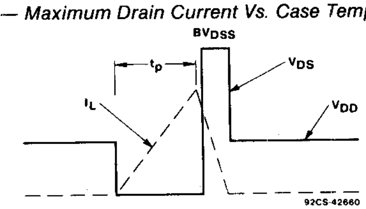


Fig. 15 — Unclamped Energy Waveforms

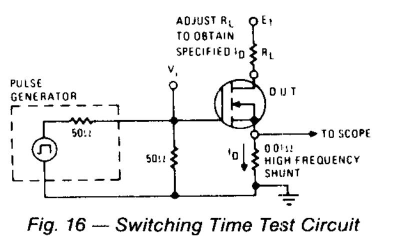


Fig. 16 — Switching Time Test Circuit

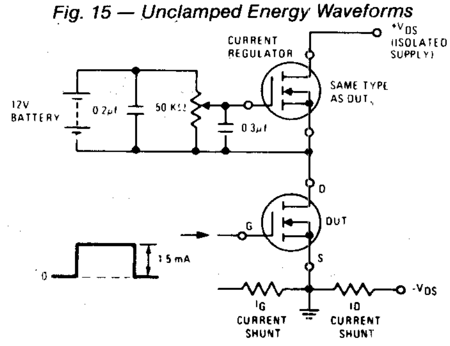


Fig. 17 — Gate Charge Test Circuit

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