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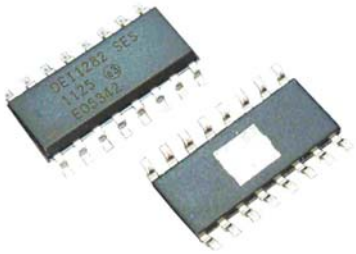
DEI1282
8CH BIT PROGRAMMABLE GND/OPN & 28V/OPN DISCRETE INTERFACE IC

FEATURES



- Eight discrete inputs
  - Individually configurable as either GND/OPEN or 28V/OPEN(GND) inputs.
  - Input threshold and hysteresis per AirBus ABD0100H specification.
    - GND/OPEN mode: 4.5V/10.5V threshold, 3V hysteresis
    - 28V/OPEN mode: 6V/12V threshold, 3V hysteresis
  - 1mA input current to prevent dry relay contacts.
  - Internal isolation diodes
  - Inputs protected from Lightning Induced Transients per DO160F, Section 22, Cat A3 and B3
  - Withstands inadvertent application of 115VAC/400Hz power
  - Built-in Test (BIT) to test internal circuits including input comparator
- Serial I/O interface to read data register and write configuration register
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 8.6MHz Max Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3V +/-5%
- Analog Supply Voltage (VDD): 12V to 16.5V
- 16L SOIC EP package

PIN ASSIGNMENTS

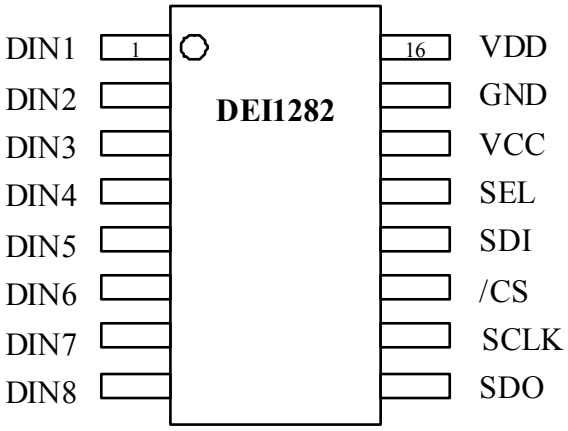


Figure 1 DEI128 Pin Assignment (16 Lead SOIC)

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FUNCTIONAL DESCRIPTION

DEI1282 is an eight-channel discrete-to digital interface IC implemented in a High Voltage Dielectric Isolated technology. It senses eight discrete signals of the type commonly found in avionic systems and converts them to serial logic data. Each input can be individually configured as either GND/OPEN or 28V/OPEN format input via a serial data input. The discrete data is read from the device via an eight-bit serial shift register with 3-state output. This serial interface is compatible with the industry standard Serial Peripheral Interface (SPI) bus.

The discrete inputs are implemented with High Voltage technology to provide immunity to Lightning Induced transients (DO160F Level 3) without the need for additional protection components.

The on-chip Built-in Test (BIT) feature provides a Test Mode which provides a means to inject a test signal into each input comparator without interfering with the discrete input signals. The test coverage includes each DIN comparator as well as the digital logic and IO.

Table 1 Pin Descriptions

PINS	NAME	DESCRIPTION
1-8	DIN[1:8]	Discrete Inputs. Eight discrete signals which can be individually configured as either GND/OPEN or 28V/OPEN format inputs.
9	SDO	Logic Output. Serial Data Output. This pin is the output from MSB (Bit 8) of the selected shift register (Data/Configuration). It is clocked by the rising edge of SCLK. This is a 3-state output enabled by /CS.
10	SCLK	Logic Input. Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into Bit 0 of the selected shift register. The selected shift register is shifted from Bit 1 to Bit 8. Bit 8 of the selected shift register is driven on SDO.
11	/CS	Logic Input. Chip Select. A low level on this input enables the SDO 3-state output and the selected shift register. A high level on this input forces SDO to the high impedance state and disables the shift registers so SCLK transitions have no effect. When the Data Register is selected, a high-to-low transition causes the Discrete Input data to be loaded into the Data Register. When the Configuration Register is selected, a low-to-high transition causes the Serial Configuration Register data to be loaded into the parallel configuration outputs.
12	SDI	Logic Input. Serial Data Input. Data on this input is shifted into the LSB (Bit 1) of the selected shift register on the rising edge of the SCLK when /CS input is low.
13	SEL	Logic Input. Selects between the Data Register and Configuration Register. H = DATA, L = CONF.
14	VCC	Logic Supply Voltage. 3.3V+/-5%
15	GND	Logic/Signal Ground
16	VDD	Analog Supply Voltage. 12V to 16.5V

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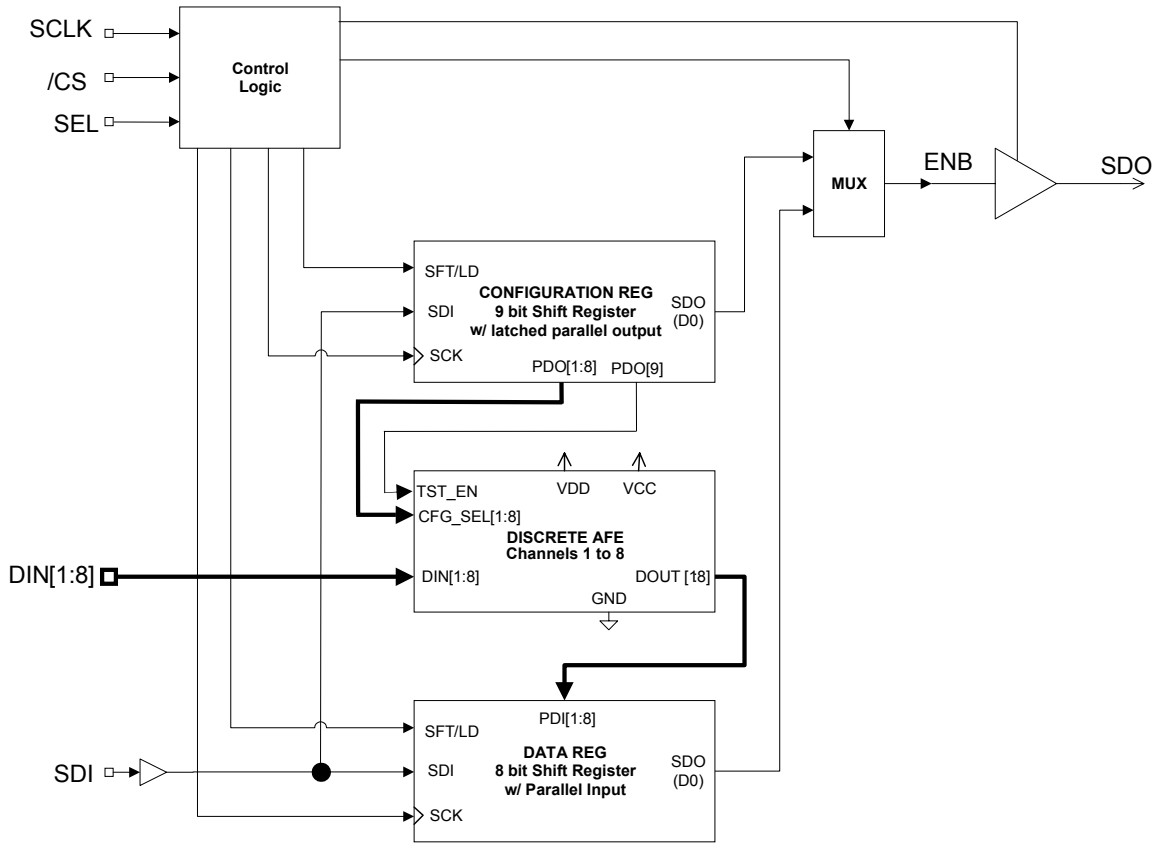


Figure 2 Function Diagram

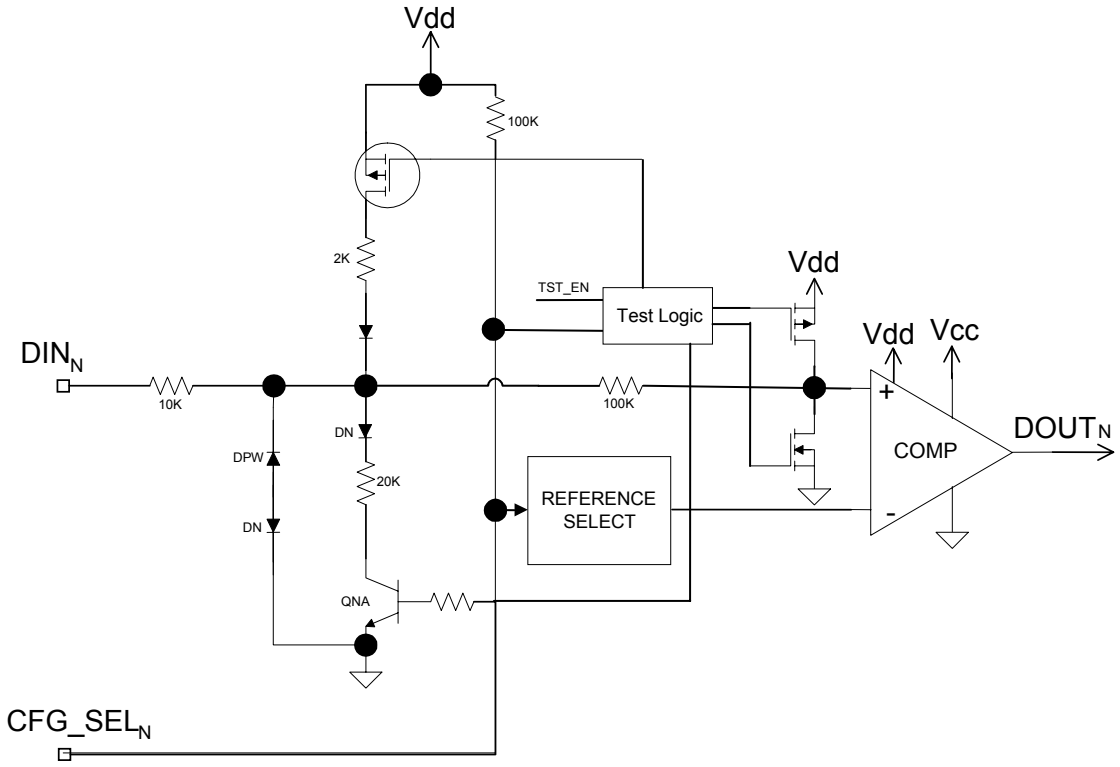


Figure 3 Discrete AFE Function Diagram

Table 2 Truth Table

Serial Interface Operation						
SEL	**/CS**	**SCLK**	**SDI**	**DIN[1:8]**	**SDO**	**Description**
X	H	X	X	X	HI Z	Not Selected
H	↓	L	X	Valid	DIN[8]	DR[1:8]← DIN[1:8]
H	L	↑	DR[1]	X	DR[8]	DR[n+1] ← DR[n], DR[1] ← SDI
L	L	↑	CR[1]	X	CR[8]	CR[n+1] ← CR[n], CR[1] ← SDI
L	↑	L	X	X	HI Z	CL[1:8]← CR[1:8]

Legend:
DR = Data Register
CR = Configuration Register
CL = Configuration Latch
X = Don't Care

DIN [1:8] Discrete AFE

The Discrete Input Analog Front End circuit function is represented in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to a comparator with hysteresis. When the input is configured for GND/OPEN operation, the pull-up resistor and diode are enabled and comparator threshold voltage is selected. When the input is configured for 28V/OPEN operation, the pull-down resistor is enabled and the comparator is appropriately configured. Prior to configuration (after power up), neither pull-up nor pull-down is enabled and the AFE presents a high impedance (Hi-Z).

Some notable features are:

- The input threshold voltage and hysteresis:
  - 28V/OPEN
    - Low-to-high threshold voltage: 12V > Vth > 10.5V.
    - High-to-low threshold voltage: 6V < Vth < 7.5V.
    - Hysteresis: Vhys > 3V.
  - GND/OPEN
    - Low-to-high threshold voltage: 10.5V > Vth > 9V.
    - High-to-low threshold voltage: 4.5V < Vth < 6V.
    - Hysteresis: Vhys > 3V.
- The input current is ~ 1mA. This current will prevent a "dry" relay contact.
- Input noise immunity is maximized with a combination of voltage hysteresis and use of a slow input voltage comparator
- The inputs can withstand continuous input voltages of 49V, lightning transient voltages per DO160 Level 3 pin injection tests, and survive inadvertent application of 115VAC/400Hz.

Data Register

The 8-bit Data Register is a "parallel-input, serial-output" register that samples the input channels and reads-out the data to the Serial Data Output. The register is read via the SDO output as described in Figure 4 and Figure 5. A low DIN input level results in a Logic 0, and a high input level results in a Logic 1.

Configuration Register

The 9-bit Configuration Register (CR) is a "serial-input, parallel-output with data latch" register that individually configures each AFE input as either GND/OPEN or 28V/OPEN format. (CR[n]: 0 sets DIN[n] to 28V/OPEN mode (pull-down); CR[n]: 1 sets DIN[n] to GND/OPEN mode (pull-up)). The register is reset to 0's at Power Up and the AFE inputs are forced in to high impedance mode until the CR is programmed. (see Power Up Initialization). Bit 9 is used to enable or disable Built-in Test (see BIT Operation). The register is programmed via the serial data input as described in Figure 6 and Figure 7.

Serial Interface

The DEI1282 incorporates a serial IO interface for programming the Discrete Input configuration and for reading the Discrete Input status. Refer to

Figure 2. The interface is SPI compatible and consists of /CS, SEL, SCLK, SDO, and SDI signals. Figures 4 – 7 depict the Data Read sequence and Configuration Write sequence for both a single device and dual "daisy chained" devices; refer to Figure 16 for connection details.

Power Up Initialization

The DEI1282 incorporates an on-chip power-up reset (POR) circuit and logic to force the DIN inputs to a high impedance state at power up; the AFE pull-up and pull-down circuits are disabled. POR monitors the VCC logic supply and forces the AFE to the high impedance state while VCC is stabilizing. It remains high impedance until the Configuration Register is programmed by the first Write Configuration Register cycle when the pull-up or pull-down state is defined.

The POR rising Vcc threshold is ~2.5V with ~0.4V of hysteresis. The POR includes a ~200us delay from the Vcc threshold to reset output; the Configuration Register ignores attempts to program it during this POR delay time.

The POR will reset when there is sufficient voltage sag on Vcc. When VCC drops below ~2.0V for ~9us, POR will activate, the Configuration and Data Registers will reset to "0", and the AFEs (DIN's) are set to Hi-Z.

BIT Operation

Bit 9 of the Configuration Register (CR) is used to enable or disable Built-in Test (1 = BIT enabled, 0 = Normal). When BIT is enabled, each channel configuration bit value is used to drive a test stimulus on the respective channel comparator (see Figure 3). Thus all channels can be tested by setting the BIT mode, programming test stimulus patterns into the CR, and reading the results from the DR. The DIN inputs are placed in Hi-Impedance mode (pull up and pull down switches are OFF) during test mode, so the test does not interfere with the DIN signals. The BIT test stimulus is isolated from the DIN pin by 100KΩ.

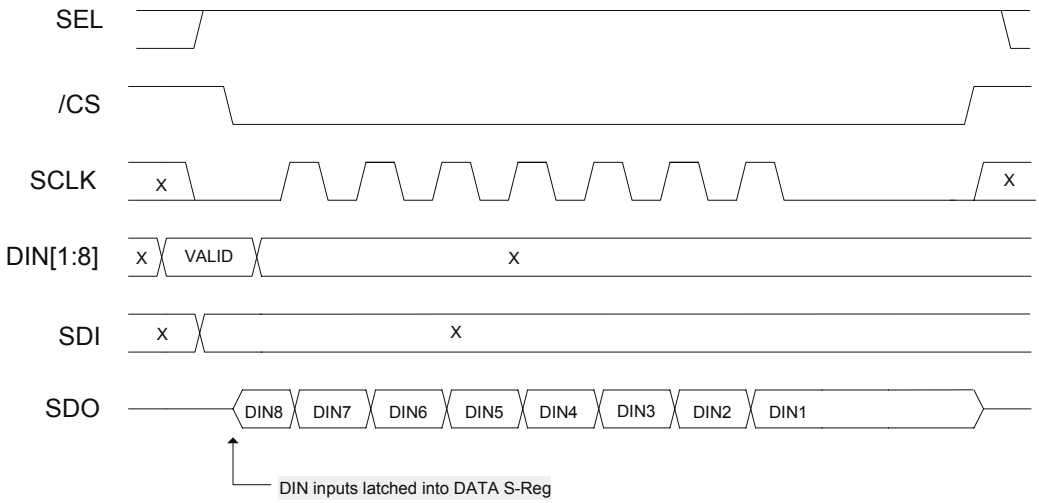


Figure 4 Read Data Register

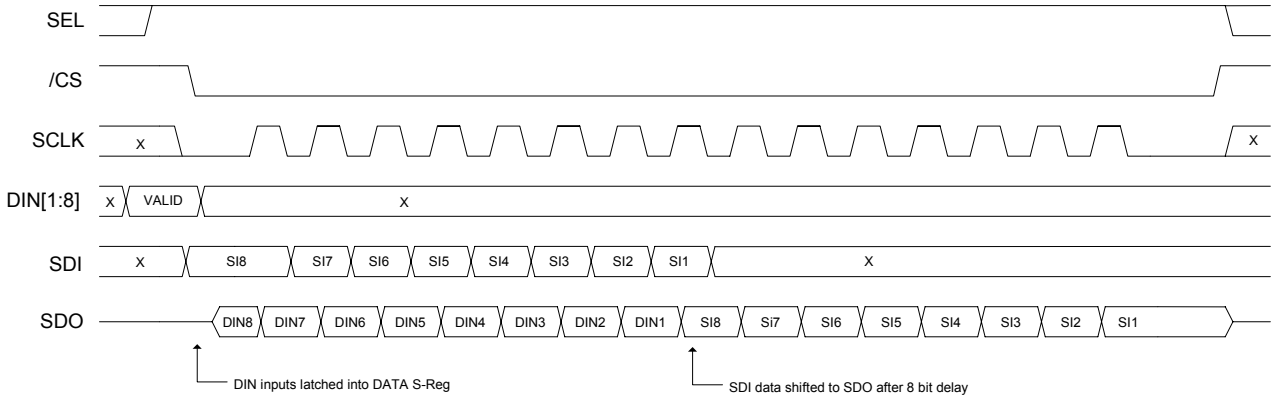


Figure 5 Read Data Register, 16 Bit Daisy Chain (See Figure 16**)**

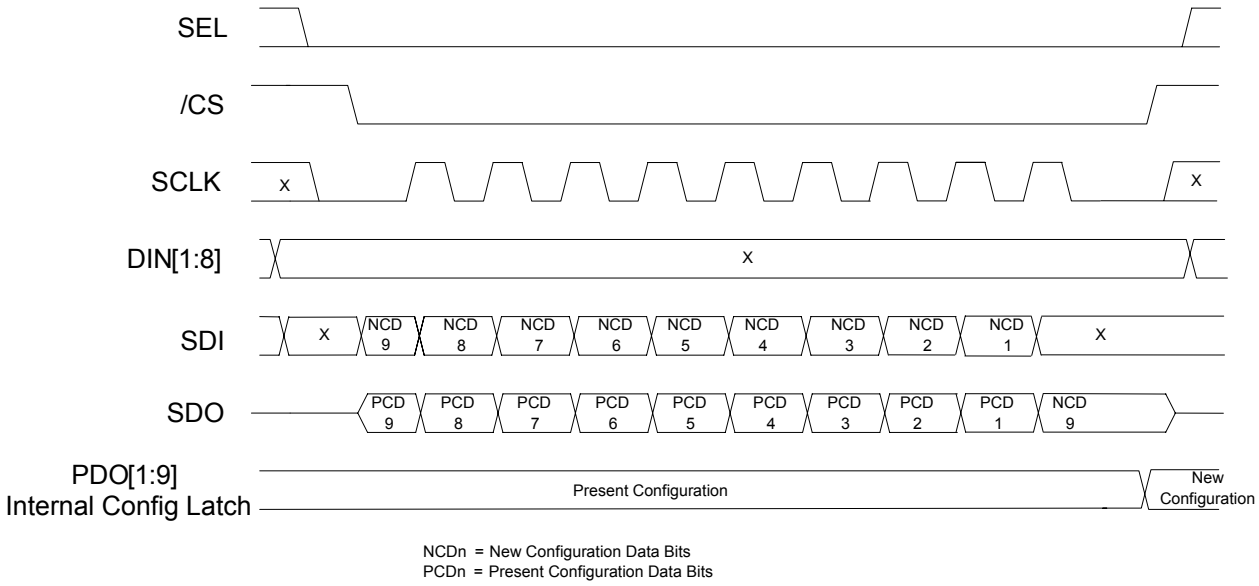


Figure 6 Write Configuration Register

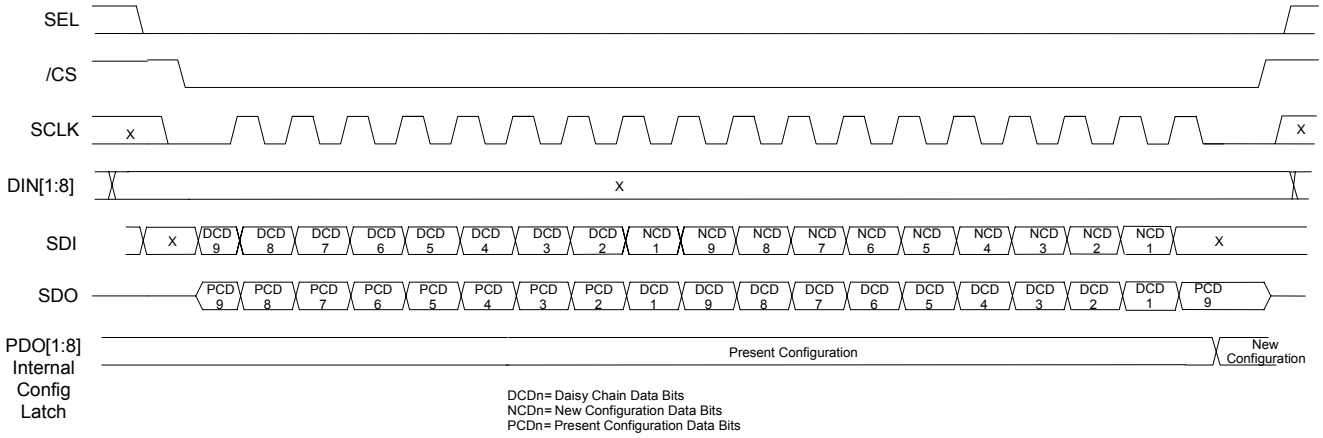


Figure 7 Write Configuration Register, 18 bit Daisy Chain (See Figure 16**)**

LIGHTNING TRANSIENT IMMUNITY

The DIN inputs are designed to survive lightning induced transients as defined by RTCA DO160F, Section 22, Cat A3 and B3, Waveforms 3, 4 and 5A, Level 3. Contact factory for lightning test report.

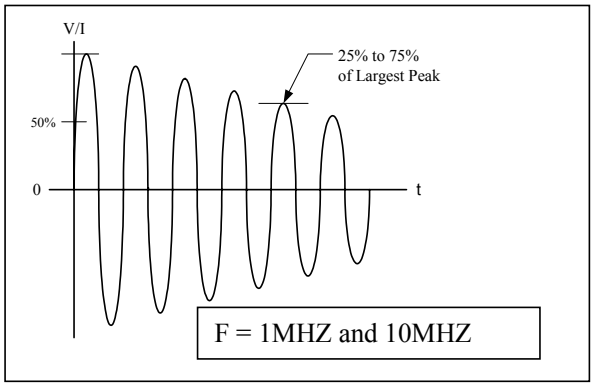


Figure 8 Voltage / Current Waveform 3

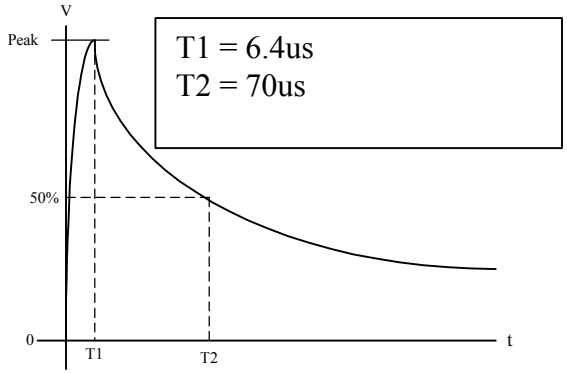


Figure 9 Voltage Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600V / 24A => 25 Ω
- Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ω
- Waveform 5A Voc / Isc = 300V / 300A => 1 Ω
- Waveform 5A Voc / Isc = 500V / 500A => 1 Ω

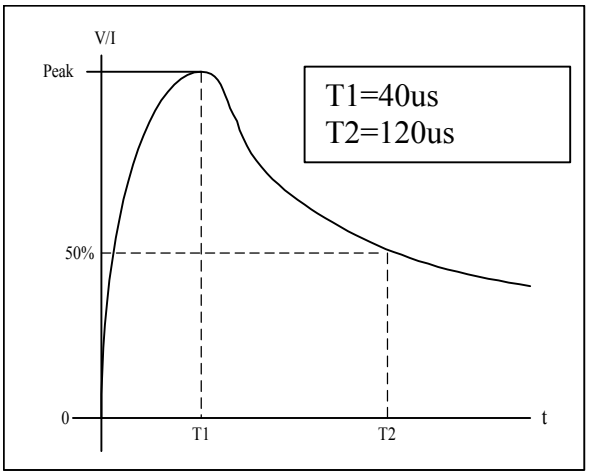


Figure 10 Voltage / Current Waveform 5A

INADVERTANT SHORT TO 115VAC POWER

The DIN inputs are able to withstand inadvertent shorts to 115VAC/400Hz aircraft power.

Contact factory for test report.

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNITS
VCC Supply Voltage		-0.3	+5.0	V
VDD Supply Voltage		-0.3	18	V
Operating Temperature				
Exposed pad soldered to heat sink		-55	+125	°C
Storage Temperature				
Plastic Package		-55	+150	°C
Input Voltage				
DIN[1:8]	Continuous	-10	+49	Vdc
	DO160F, Waveform 3, Level 3	-600	+600	Vpk
	DO160F, Waveform 4 and 5, Level 3	-300	+300	Vpk
	DO160F, Abnormal Surge Voltage, 100ms		80	Vpk
Logic Inputs		-1.5	VCC + 1.5	V
DOUT		-0.5	VCC + 0.5	V
Power Dissipation @ 125°C, Steady state				
16L SOIC			0.63	W
Junction Temperature:				
Tjmax, Plastic Packages			150	°C
ESD per JEDEC A114-A Human Body Model				
Logic and Supply pins			2000	V
DIN pins			1000	V
Peak Body Temperature (10 sec duration)			260	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. Voltages referenced to Ground

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	3.3V±5% 12V to 16.5V
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[1:8]	0 to 49V
Operating Temperature Plastic	Ta	-55ºC to 125ºC

Table 5 DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (1)	MIN LIMIT	NOM	MAX LIMIT	UNIT
Logic Inputs/Outputs						
V_{IH}	HI level input voltage	VCC = 3.3V	2.0			V
V_{IL}	LO level input voltage	VCC = 3.3V			0.8	V
V_{Ihst}	Input hysteresis voltage, SCLK input	(3)	50			mV
V_{OH}	HI level output voltage	IOUT = -20uA	VCC – 0.1			V
		IOUT = -4mA, VCC = 3V	2.4			V
V_{OL}	LO level output voltage	IOUT = 20uA			0.1	V
		IOUT = 4mA, VCC = 3V			0.4	V
I_{IN}	Input leakage	VIN = VCC or GND	-10		10	uA
I_{OZ}	3-state leakage current	Output in Hi Impedance state. VOUT = VIHmin, VILmax	-10		10	uA
Discrete Inputs, Configured as Ground/Open (internal pull-up)						
V_{IH}	HI level input voltage		10.5		49	V
VT_{LH}	Input threshold, LO to HI		9.0		10.5	V
R_{IH}	HI level Din-to-GND resistance	Resistor from DIN to GND to guarantee HI input condition.	50K			Ω
I_{IH}	HI level input current	VIN = 28V, VDD = 15V VIN = 49V, VDD = 15V		17 45	100 250	uA uA
V_{IL}	LO level input voltage		-4.0		4.5	V
VT_{HL}	Input threshold, HI to LO		4.5		6.0	V
R_{IL}	LO level Din-to-GND resistance	Resistor from DIN to GND to guarantee LO input condition.			500	Ω
I_{IL}	LO level input current	VIN = 0V, VDD = 15V	-0.8	-1.0	-1.8	mA
V_{Ihst}	Input hysteresis voltage		3			V
Discrete Inputs, Configured as 28V/Open (internal pull-down)						
V_{IH}	HI level input voltage		12.0		49	V
VT_{LH}	Input threshold, LO to HI		10.5		12	V
I_{IH}	HI level input current	VIN = 28V, VDD = 15V	0.6	0.8	1.35	mA
V_{IL}	LO level input voltage		-4		6.0	V
VT_{HL}	Input threshold, HI to LO		6.0		7.5	V
I_{IL}	LO level input current	VIN = 1V, VDD = 15V			50	uA
V_{Ihst}	Input hysteresis voltage		3			V
Power Supply						
ICC	Max quiescent logic supply current	VIN(logic) = VCC or GND VIN[1:8] = open		1.8	3	mA
IDD	Max quiescent analog supply current	VIN(logic) = VCC or GND Ground/Open Mode, VIN[1:8] = Open VIN[1:8] = GND		15 22	24 33	mA

Notes:

1. Ta = -55ºC to 125ºC., VDD = 12V to 16.5V, VCC = 3.3V+/-5% unless otherwise noted. For worst test condition, VCC=3V is used for convenient.
2. Current flowing into device is '+'. Current flowing out of device is '-'. Voltages are referenced to Ground.
3. Guaranteed by design. Not production tested.

Table 6 AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (6,7)	MIN LIMIT	MAX LIMIT	UNIT
f_{MAX}	SCLK frequency.	50% duty cycle (5)	0.1	8.6	MHz
t_W	SCLK pulse width.	(5)	50		ns
t_{su1}	Setup time, SCLK low to /CS↓.		30		ns
t_{h1}	Hold time, /CS↓ to SCLK↑.		25		ns
t_{su2}	Setup time, DIN valid to /CS↓.	(5)	500		ns
t_{h2}	Hold time, /CS↓ to DIN not valid.		15		us
t_{su3}	Setup time, SDIN valid to SCLK↑.		25		ns
t_{h3}	Hold time, SCLK↑ to SDIN not valid.		25		ns
t_{su4}	Setup time, SEL valid to /CS↓.		30		ns
t_{h4}	Hold time, SEL valid to /CS↑.		25		ns
t_{p1}	Propagation delay, /CS↓ to DOUT valid.	(1)		105	ns
t_{p2}	Propagation delay, SCLK↑ to DOUT valid.	(1)		90	ns
t_{p3}	Propagation delay, /CS↑ to DOUT HI-Z.	(1) (2) (3)		80	ns
t_{p4}	Delay time between /CS active.	(5)	20		ns
C_{in}	Maximum logic input pin Capacitance.	(5)		10	pF
C_{out}	Maximum SDO pin capacitance, output in HI-Z state.	(5)		15	pF

Notes:
1. SDO loaded with 50pF to GND.
2. SDO loaded with 1KΩ to GND for Hi output, 1KΩ to VCC for Low output.
3. Timing measured at 25%VCC for "0" to Hi-Z, 75%VCC for "1" to Hi-Z.
4. Sample tested on lot basis.
5. Guaranteed by design. Not production tested.
6. Ta = -55ºC to 85 or 125ºC, VCC = 3V, VDD = 15V, VIL = 0V, VIH = VCC unless otherwise noted.
7. Measurements made at 50%VCC.
8. Guaranteed by design. Not production tested.

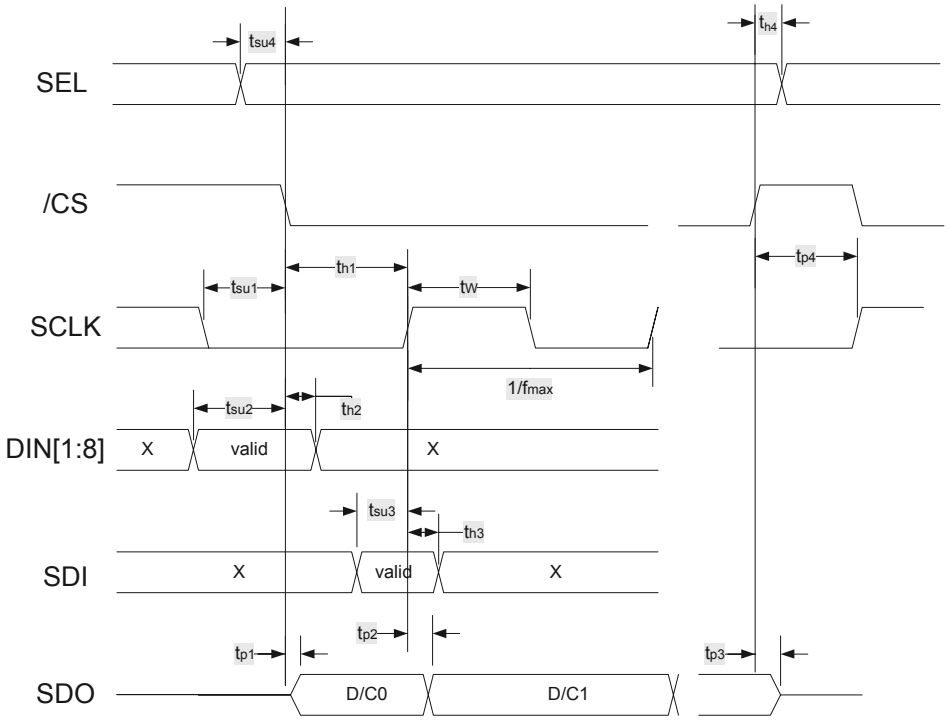


Figure 11 Switching Waveforms

APPLICATION INFORMATION

Discrete Input Filtering

The DEI1282 Analog Front End provides a moderate level of noise immunity via a combination hysteresis and limited bandwidth. The Hysteresis is 3V minimum and the comparator bandwidth is approximately 10MHz.

Many applications provide additional noise immunity by means of debounce/filtering in software or in digital circuitry (i.e.: FPGA). Common input debounce techniques are readily found with a web search of the term "software debounce" and range from simple detectors of two or more sequential stable readings to FIR filters emulating RC time constants.

Input Current Characteristics

Figures 12-15 depicts the DIN Input Current vs. Voltage characteristics for the various operating and non-operating modes. Measurements are at Room temperature.

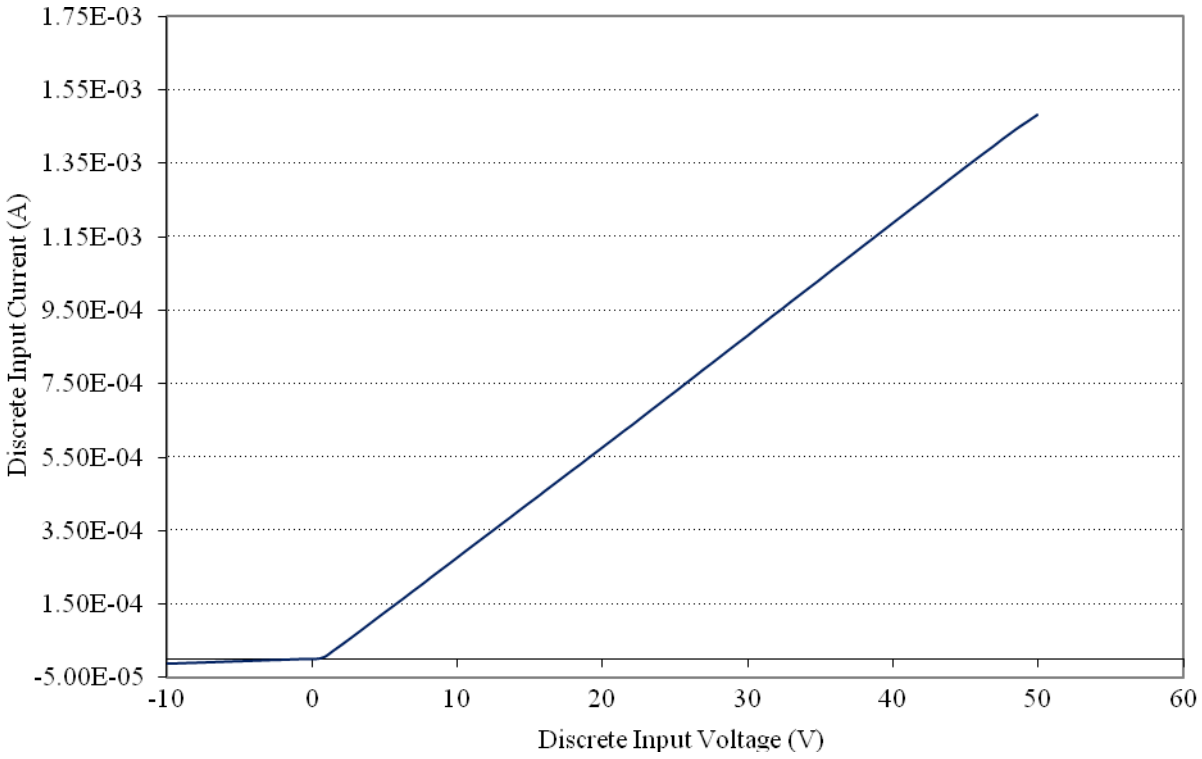


Figure 12 28V/Open Mode Input IV Characteristics (VDD = 15V)

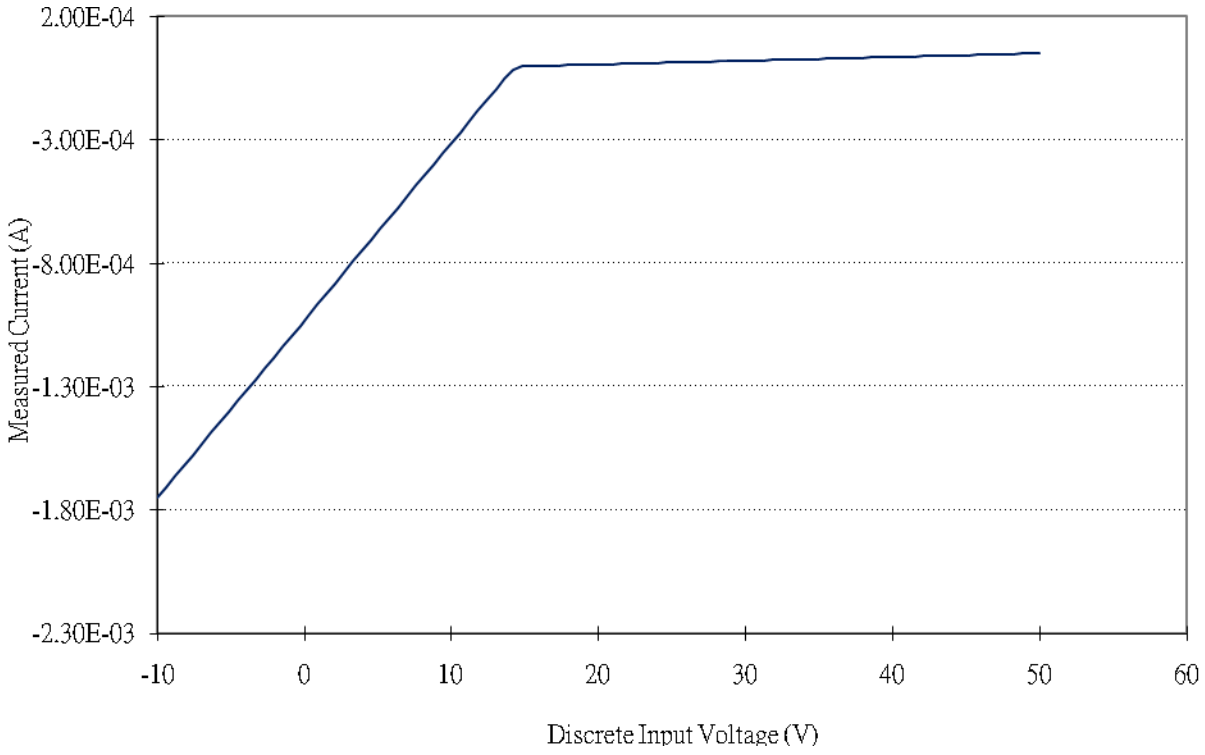


Figure 13 GND/OPEN Mode Input IV Characteristics (VDD = 15V)

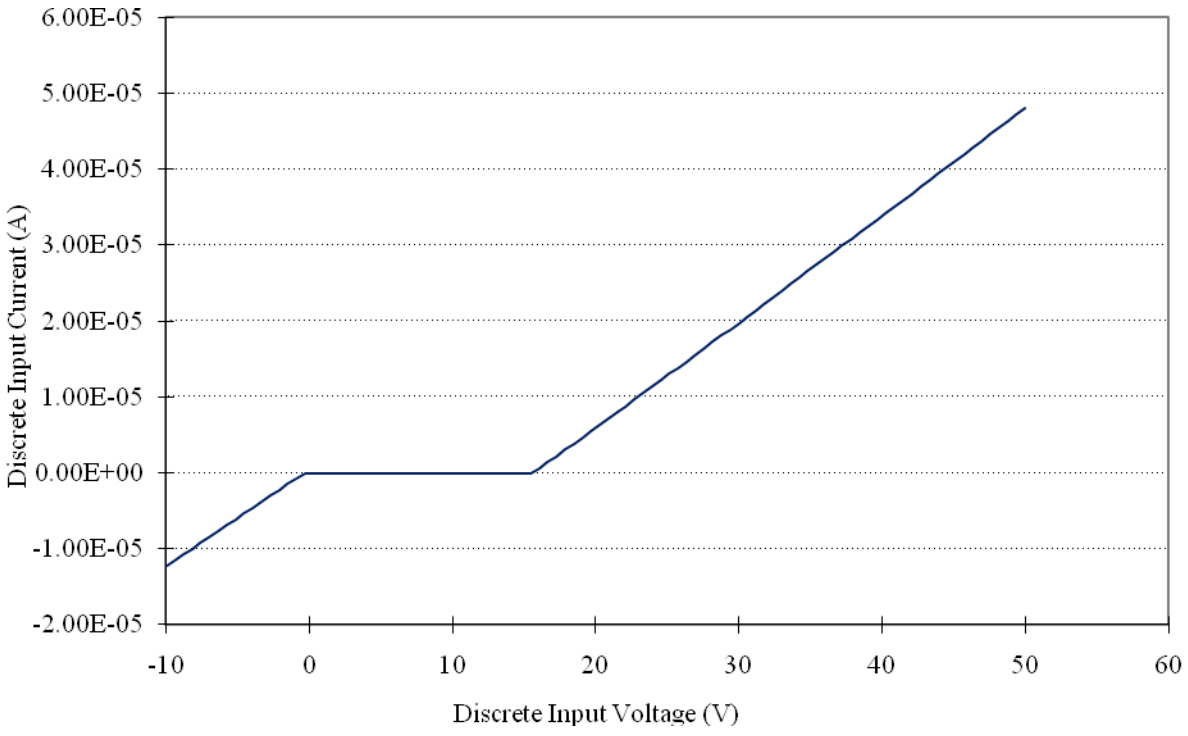


Figure 14 Hi-Z (Unconfigured and BIT) Mode Input IV Characteristics (VDD = 15V)

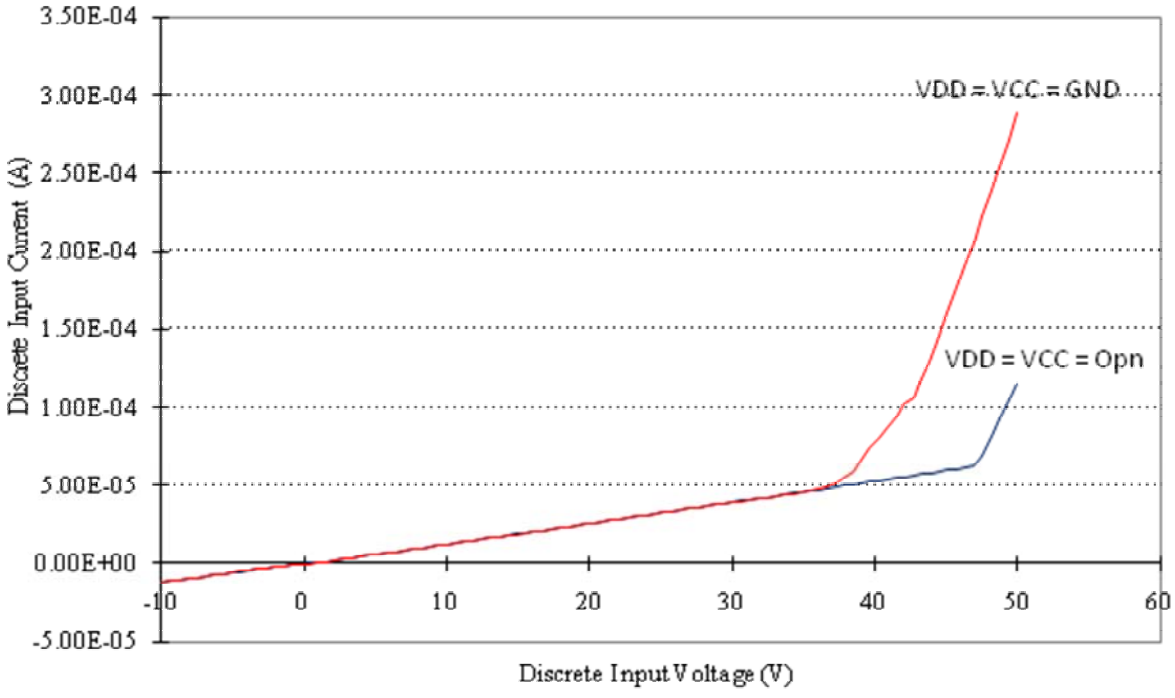


Figure 15 VDD = VCC= GND and VDD = VCC = Open Input IV Characteristics

Daisy Chain Connection

Multiple DEI1282 ICs can be connected as daisy chain. Figure 16 shows three DEI1282 in series. The critical timing is Tsu3 (see Fig 11), minimum SDIN valid to SCLK setup time.

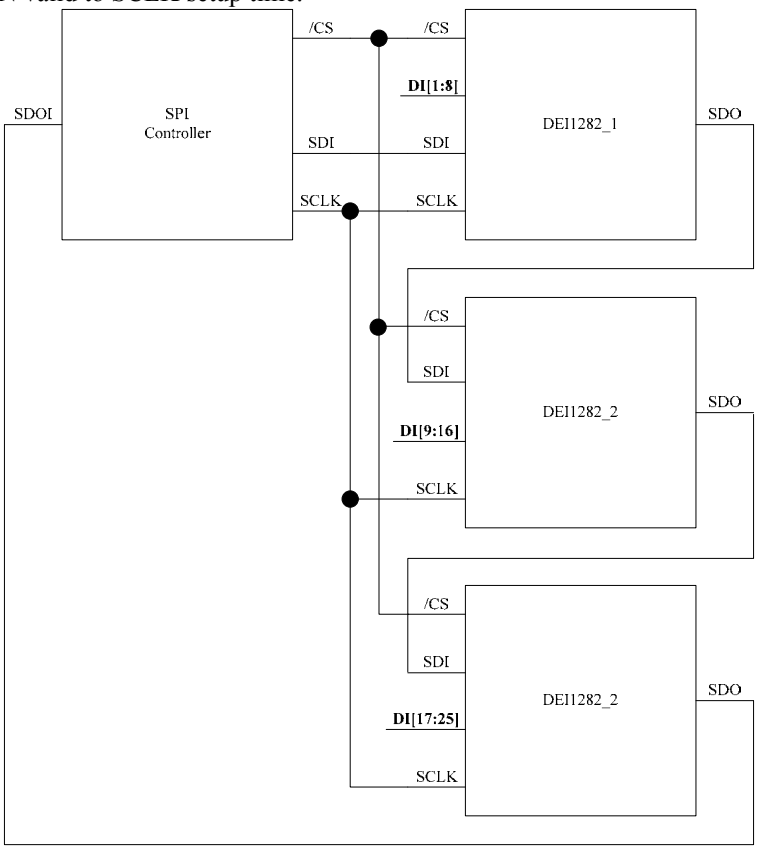


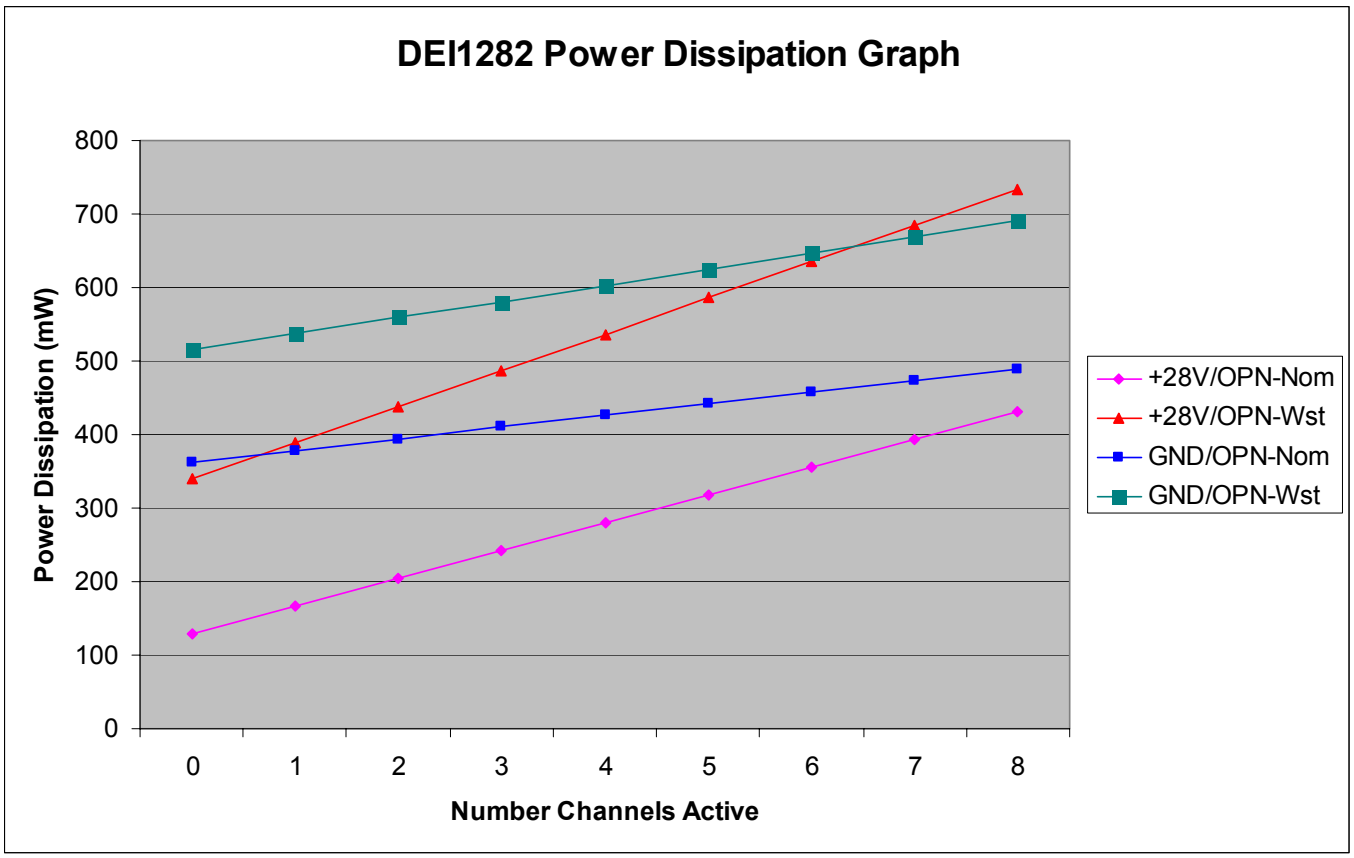
Figure 16 Example connection of 3 DEI1282 connected as daisy chain

Package Power Dissipation

The DEI1282 power dissipation varies with channel configuration and operating conditions. Figure 17 shows the device package power dissipation for various conditions. This includes the contributions from Supply currents and Input currents. The four curves are as follows:

Table 7 Legend for Power Dissipation Curves

CURVE ID	SUPPLY VOLTAGE, TEMPERATURE, IC VARIATION
+28V/OPEN-Nom	3.3V, 12V / 27ºC / typical IC parameters
+28V/OPEN-Wst	3.3V, 16.5V / 125ºC / Worst case IC parameters
GND/OPEN-Nom	3.3V, 12V / 27ºC / typical IC parameters
GND/OPEN-Wst	3.3V, 16.5V / 125ºC / Worst case IC parameters



Notes: The active channels are forced to Ground for GND/OPN type and forced to 28V for 28V/OPN type.

Figure 17 Power Dissipation for Various Conditions

PACKAGE DESCRIPTION - 16L Narrow Body EP SOIC

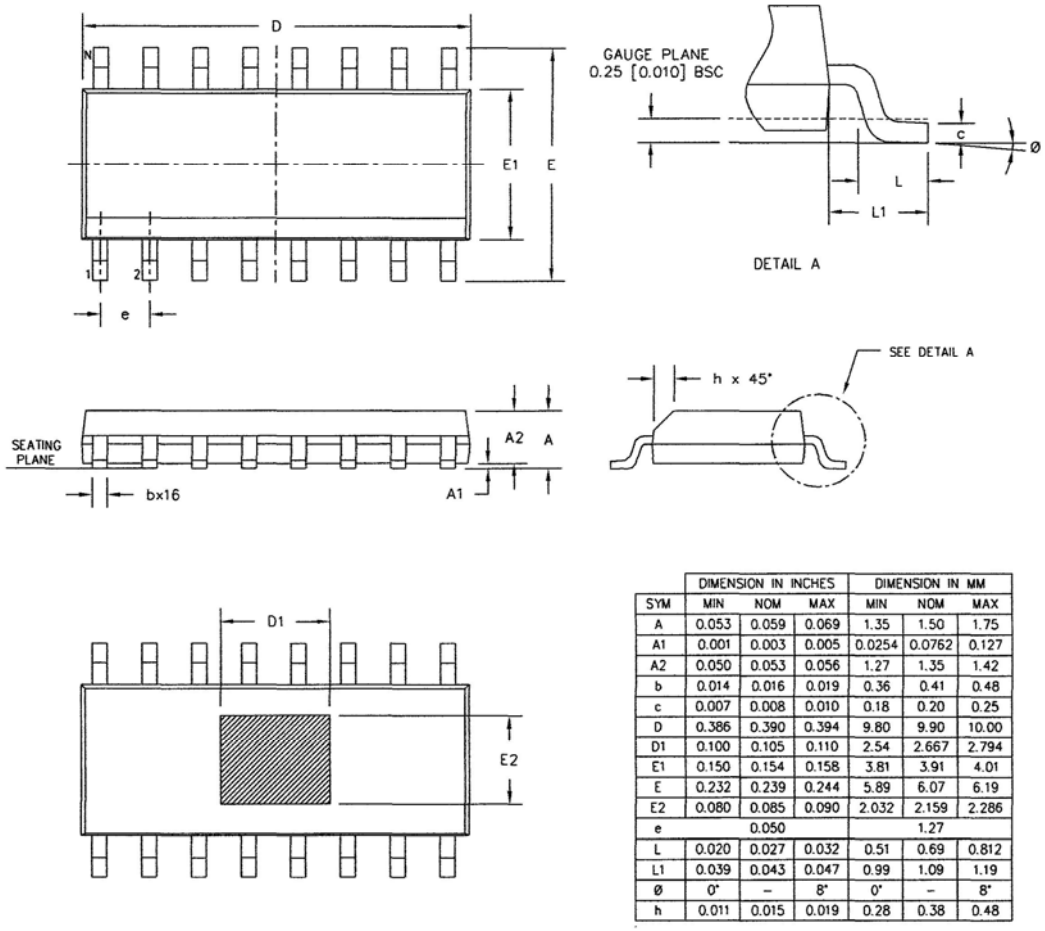
Table 8 Package Information

Package Type	Package Ref	Θjc/ Θja (°C/W) /1	JEDEC Moisture Sensitivity Level	Lead Finish / JEDEC Pb-Free Code	Pb Free Designation	JEDEC MO
16L SOIC NB SnPb	16 EP SOICN	~10 / ~40	MSL 1 / 260°C	85/15 SnPb plate na	Not Pb-free	MS-012-AC
16L SOIC NB Matte Sn RoHS	16 EP SOICN G	~10 / ~40	MSL 1 / 260°C	100% Matte Sn e3	RoHS	MS-012-AC

Notes:
1. Mounted on 4 layer PCB with exposed pad soldered to PCB land with thermal VIAs to internal GND plane

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the IC package**.** Use maximum trace width on all power and signal connections at the IC; these traces serve as heat spreaders which improve heat flow from the IC leads**.**

The exposed pad on the bottom of the SOIC package must be soldered to a heat-spreader land pattern on the PCB. The IC exposed pad is electrically isolated, but must be connected to some potential on the PCB, typically Ground or Vcc . Maximize the PCB land size by extending it beyond the IC outline if possible. A grid of thermal VIAs, which drop down and connect to the buried copper plane(s), should be placed under the heat-spreader land. A typical VIA grid is 12mil plated holes on a 50mil pitch. Use as many VIAs as space allows. VIAs should be plugged to prevent voids being formed between the exposed pad and PCB heat-spreader land due to solder escaping by the capillary effect. Wicking can be avoided by tenting the VIAs with solder mask.



	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	0.059	0.069	1.35	1.50	1.75
A1	0.001	0.003	0.005	0.0254	0.0762	0.127
A2	0.050	0.053	0.056	1.27	1.35	1.42
b	0.014	0.016	0.019	0.36	0.41	0.48
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.386	0.390	0.394	9.80	9.90	10.00
D1	0.100	0.105	0.110	2.54	2.667	2.794
E1	0.150	0.154	0.158	3.81	3.91	4.01
E	0.232	0.239	0.244	5.89	6.07	6.19
E2	0.080	0.085	0.090	2.032	2.159	2.286
e		0.050			1.27	
L	0.020	0.027	0.032	0.51	0.69	0.812
L1	0.039	0.043	0.047	0.99	1.09	1.19
Ø	0°	–	8°	0°	–	8°
h	0.011	0.015	0.019	0.28	0.38	0.48

Note: The bottom thermal contact (exposed pad) is electrically isolated.

Figure 18 16 Lead Narrow Body EP SOIC Outline

ORDERING INFORMATION

Table 9 Ordering Information

Part Number	Marking	Package (1)	Burn In	Temperature
DEI1282-SES	DEI1282-SES	16 EP SOIC	No	-55ºC / 85ºC
DEI1282-SMS	DEI1282-SMS	16 EP SOIC	No	-55ºC / 125ºC
DEI1282-SES-G	DEI1282-SES-G / e3	16 EP SOIC G	No	-55ºC / 85ºC
DEI1282-SMS-G	DEI1282-SMS-G / e3	16 EP SOIC G	No	-55ºC / 125ºC

Notes:
1. Refer to Table 8