Semiconductor Corporation

CS8005

Advanced Ethernet Data Link Controller

Features

- High Throughput
  - Supports Full 10M BPS Data Rate
  - Back-to-Back Packets
- 64 K-Byte Local Packet Buffer
  - Provides refresh for DRAMs
  - Off-loads host bus
- Conforms to ISO/ISEE 802.3 Standard
- Flexible Bus Interface
  - Intel and Motorola bus modes
  - I/O, string move, DMA access
  - Memory or I/O mapped
  - 8 or 16 bit bus width
- Recognizes One to Six Receive Addresses, Specific, Multicast or Broadcast
- Advanced Error Correction and Handling
  - Automatic re-transmit after a collision
  - Automatically discards bad packets

General Description

The CS8005 has five major blocks: the Transmitter, Receiver, Buffer Controller, Bus Interface and Status and Command Register.

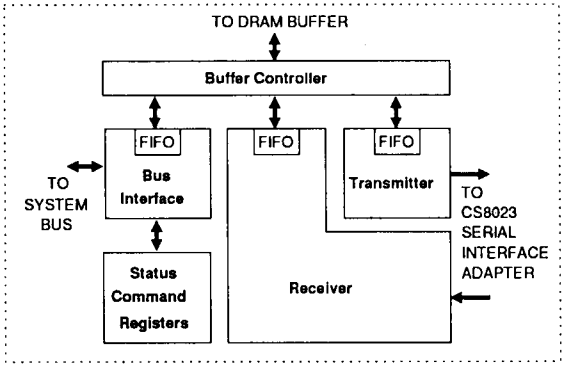
The CS8005 supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, CRC generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses including multicast/broadcast addresses.

The Buffer Controller manages a 64K byte local packet buffer. This block provides arbitration and control for four memory ports: the transmitter, the receiver, the bus interface and an internal DRAM refresh generator. Received packets are temporarily stored until the system either reads or disposes of them, and packets placed there by the system are held for transmission over the link.

The Bus Interface interfaces to the system bus and provides access to internal configuration and status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of Packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called DMA FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the Transmitter or Receiver or refreshing the DRAM.

ORDERING INFORMATION:

CS8005-L	68-pin PLCC



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