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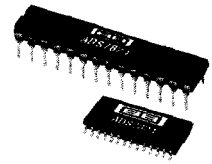


ADS7824

www.burr-brown.com/databook/ADS7824.html

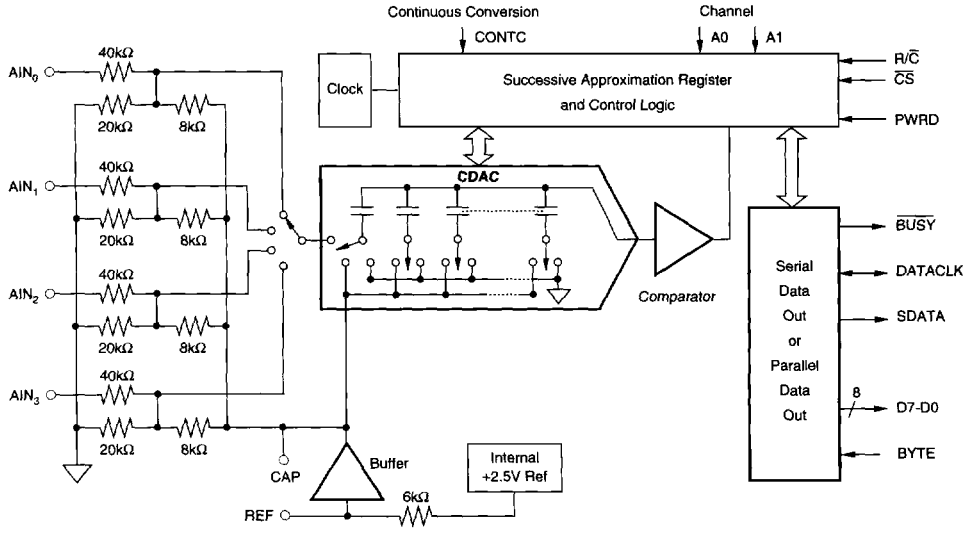
4 Channel, 12-Bit Sampling CMOS A/D Converter

FEATURES

- 25µs max SAMPLING AND CONVERSION
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7825
- PARALLEL AND SERIAL DATA OUTPUT
- 28-PIN 0.3" PLASTIC DIP AND SOIC
- ±0.5 LSB max INL AND DNL
- 50mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- ±10V INPUT RANGE, FOUR CHANNEL MULTIPLEXER
- CONTINUOUS CONVERSION MODE

DESCRIPTION

The ADS7824 can acquire and convert 12 bits to within ±0.5 LSB in 25µs max while consuming only 50mW max. Laser-trimmed scaling resistors provide the standard industrial ±10V input range and channel-to-channel matching of ±0.1%. The ADS7824 is a low-power 12-bit sampling A/D with a four channel input multiplexer, S/H, clock, reference, and a parallel/serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. The 28-pin ADS7824 is available in a plastic 0.3" DIP and in a SOIC, both fully specified for operation over the industrial –40°C to +85°C range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{S1} = V_{S2} = V_S = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7824P, U			ADS7824PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*[1]	Bits
ANALOG INPUT								
Voltage Range			±10V			*		V
Impedance	Channel On or Off		45.7			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Time			20			*		µs
Acquisition Time			5			*		µs
Multiplexer Settling Time	Includes Acquisition		5			*		µs
Complete Cycle (Acquire and Convert)				25			*	µs
Complete Cycle (Acquire and Convert)	CONTC = +5V			40			*	µs
Throughput Rate		40			*			kHz
DC ACCURACY								
Integral Linearity Error			±0.15	±1		*	±0.5	LSB[2]
Differential Linearity Error			±0.15	±1		*	±0.5	LSB
No Missing Codes			Guaranteed			*		
Transition Noise[3]			0.1			*		LSB
Full Scale Error[4]	Internal Reference			±0.5			±0.25	%
Full Scale Error Drift	Internal Reference		±7			±5		ppm/°C
Full Scale Error[4]				±0.5			±0.25	%
Full Scale Error Drift			±2			*		ppm/°C
Bipolar Zero Error				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Channel-to-Channel Mismatch				±0.1			±0.1	%
Power Supply Sensitivity	+4.75 < V_S < +5.25			±0.5			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range[5]	f_{IN} = 1kHz	80	90		*	*		dB
Total Harmonic Distortion	f_{IN} = 1kHz		–90	–80		*	*	dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz	70	73		72	*		dB
Signal-to-Noise	f_{IN} = 1kHz	70	73		72	*		dB
Channel Separation[6]	f_{IN} = 1kHz	90	100		*	*		dB
–3dB Bandwidth			2			*		MHz
Useable Bandwidth[7]			90			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response[8]	FS Step		5			*		µs
Overvoltage Recovery[9]			1			*		µs
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.4		V_S +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format		Parallel in two bytes; Serial				*		
Data Coding		Binary Two's Complement				*		
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_S			±5			*	µA
Output Capacitance	High-Z State			15			*	pF

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{S1} = V_{S2} = V_S = +5V ±5%, using external reference, CONTC = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7824P, U			ADS7824PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING								
Bus Access Time	PAR/$\overline{SER}$ = +5V			83			*	ns
Bus Relinquish Time	PAR/$\overline{SER}$ = +5V			83			*	ns
Data Clock	*PAR/$\overline{SER}$ = 0V*							
Internal Clock (Output only when transmitting data)	EXT/$\overline{INT}$ LOW	0.5		1.5	*		*	MHz
External Clock	EXT/$\overline{INT}$ HIGH	0.1		10	*		*	MHz
POWER SUPPLIES								
V_{S1} = V_{S2} = V_S		+4.75	+5	+5.25	*	*	*	V
Power Dissipation	f_S = 40kHz			50			*	mW
	PWRD HIGH		50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) An asterik (*) specifies same value as grade to the left. (2) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7824, one LSB is 4.88mV. (3) Typical rms noise at worst case transitions and temperatures. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) A full scale sinewave input on one channel will be attenuated by this amount on the other channels. (7) Useable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (8) The ADS7824 will accurately acquire any input step if given a full acquisition period after the step. (9) Recovers to specified performance after 2 x FS input overvoltage, and normal acquisitions can begin.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)
ADS7824P	Plastic Dip	246	–40°C to +85°C	±1	70
ADS7824PB	Plastic Dip	246	–40°C to +85°C	±0.5	72
ADS7824U	SOIC	217	–40°C to +85°C	±1	70
ADS7824UB	SOIC	217	–40°C to +85°C	±0.5	72

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: AIN_0, AIN_1, AIN_2, AIN_3	±15V
REF	(AGND2 –0.3V) to (V_S + 0.3V)
CAP	Indefinite Short to AGND2, Momentary Short to V_S
V_{S1} and V_{S2} to AGND2	7V
V_{S1} to V_{S2}	±0.3V
Difference between AGND1, AGND2 and DGND	±0.3V
Digital Inputs and Outputs	–0.3V to (V_S + 0.3V)
Maximum Junction Temperature	150°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C
Maximum Input Current to Any Pin	100mA

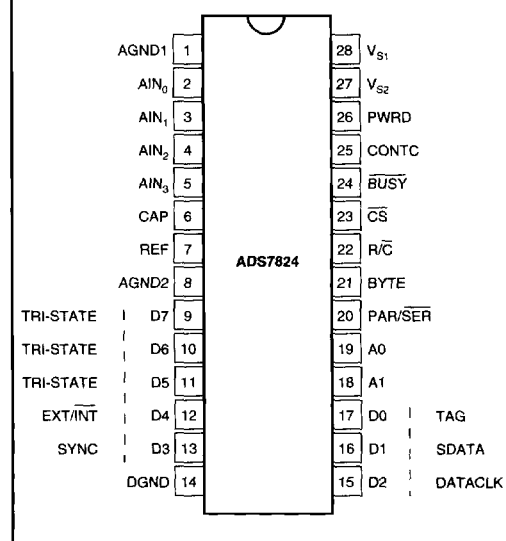
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View — DIP/SOIC



PIN ASSIGNMENTS

PIN #	NAME	I/O	DESCRIPTION
1	AGND1		Analog Ground. Used internally as ground reference point.
2	AIN_0		Analog Input Channel 0. Full-scale input range is ±10V.
3	AIN_1		Analog Input Channel 1. Full-scale input range is ±10V.
4	AIN_2		Analog Input Channel 2. Full-scale input range is ±10V.
5	AIN_3		Analog Input Channel 3. Full-scale input range is ±10V.
6	CAP		Internal Reference Output Buffer. 2.2µF Tantalum to ground.
7	REF		Reference Input/Output. Outputs +2.5V nominal. If used externally, must be buffered to maintain ADS7825 accuracy. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
8	AGND2		Analog Ground.
9	D7	O	Parallel Data Bit 7 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I.
10	D6	O	Parallel Data Bit 6 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I.
11	D5	O	Parallel Data Bit 5 if PAR/$\overline{SER}$ HIGH; Tri-state if PAR/$\overline{SER}$ LOW. See Table I.
12	D4	I/O	Parallel Data Bit 4 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, a LOW level input here will transmit serial data on SDATA from the previous conversion using the internal serial clock; a HIGH input here will transmit serial data using an external serial clock input on DATACLK (D2). See Table I.
13	D3	O	Parallel Data Bit 3 if PAR/$\overline{SER}$ HIGH; SYNC output if PAR/$\overline{SER}$ LOW. See Table I.
14	DGND		Digital Ground.
15	D2	I/O	Parallel Data Bit 2 if PAR/$\overline{SER}$ HIGH; if PAR/$\overline{SER}$ LOW, this will output the internal serial clock if EXT/$\overline{INT}$ (D4) is LOW; will be an input for an external serial clock if EXT/$\overline{INT}$ (D4) is HIGH. See Table I.
16	D1	O	Parallel Data Bit 1 if PAR/$\overline{SER}$ HIGH; SDATA serial data output if PAR/$\overline{SER}$ LOW. See Table I.
17	D0	I/O	Parallel Data Bit 0 if PAR/$\overline{SER}$ HIGH; TAG data input if PAR/$\overline{SER}$ LOW. See Table I.
18	A1	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I.
19	A0	I/O	Channel Address. Input if CONTC LOW, output if CONTC HIGH. See Table I.
20	PAR/$\overline{SER}$	I	Select Parallel or Serial Output. If HIGH, parallel data will be output on D0 thru D7. If LOW, serial data will be output on SDATA. See Table I and Figure 1.
21	BYTE	I	Byte Select. Only used with parallel data, when PAR/$\overline{SER}$ HIGH. Determines which byte is available on D0 thru D7. Changing BYTE with $\overline{CS}$ LOW and R/$\overline{C}$ HIGH will cause the data bus to change accordingly. LOW selects the 8 MSBs; HIGH selects the 4 LSBs, see Figures 2 and 3.
22	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH.
23	$\overline{CS}$	I	Chip Select. Internally OR'd with R/$\overline{C}$. With CONTC LOW and R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits if PAR/$\overline{SER}$ HIGH, or starts transmission of serial data if PAR/$\overline{SER}$ LOW and EXT/$\overline{INT}$ HIGH.
24	$\overline{BUSY}$	O	Busy Output. Falls when conversion is started; remains LOW until the conversion is completed and the data is latched into the output register. In parallel output mode, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
25	CONTC	I	Continuous Conversion Input. If LOW, conversions will occur normally when initiated using $\overline{CS}$ and R/$\overline{C}$; if HIGH, acquisition and conversions will take place continually, cycling through all four input channels, as long as $\overline{CS}$, R/$\overline{C}$ and PWRD are LOW. See Table I. For serial mode only.
26	PWRD	I	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output register. In the continuous conversion mode, the multiplexer address channel is reset to channel 0
27	V_{S2}		Supply Input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF Tantalum capacitors.
28	V_{S1}		Supply Input. Nominally +5V. Connect directly to pin 27.